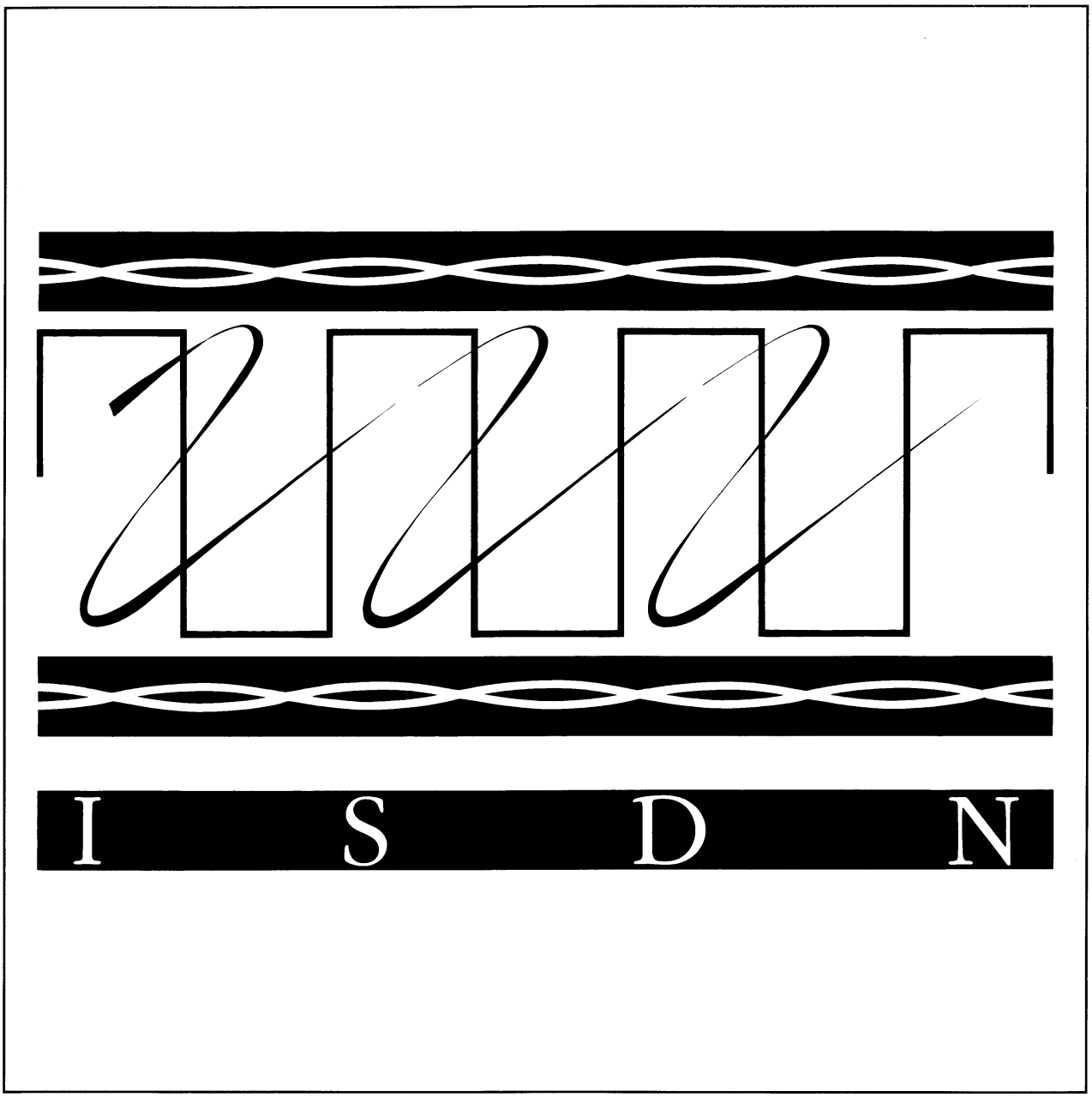
IOM-2 Interface Reference Guide

Industry Standard Bus

Advanced
Micro
Devices



Advanced Micro Devices

IOM-2 Interface Reference Guide

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CHAPTER 1

INDUSTRY STANDARD BUS—ORIGINS

The IOM™ Revision 2 (IOM-2) standard defines an industry standard serial bus for interconnecting telecommunications ICs. The standard covers line-card, NT1, and terminal architectures for ISDN and analog loop applications.

In digital telephone switches, an inter-chip communication bus is often used to connect the codec/filter ICs to the switch backbone. Typically, a separate serial bus is used between each codec/filter IC and a line-card controller IC. The line-card controller provides the connection to the switch backbone, as well as an interface to the microprocessor that controls the line card. The inter-chip bus structures that were used in this single channel per line pre-ISDN (Integrated Services Digital Network) telephone equipment are not well-suited for the 2B+D structure of ISDN.

To address this problem, four major European telephone equipment manufacturers jointly defined a new interface bus. These four companies, Alcatel, Italtel, Plessey, and Siemens invented a bus structure that satisfied the requirements of both ISDN and analog applications. The General Circuit Interface, or GCI, is an evolution of the ISDN Oriented Modular interface (IOM) invented by Siemens. The GCI was designed with the specific needs of interconnecting components on switch line cards. As such, it is not well-suited for terminal and NT1 applications. As a result, a terminal version of the interface has been designed. The terminal version has been designated the Special Circuit Interface T, or SCIT. The GCI line card and SCIT terminal bus specifications combined form the IOM Revision 2 standard (IOM-2).

CHAPTER 2

GLOBAL PICTURE

Document Organization

The specification begins with a general overview of the line-card and terminal modes, followed by a general overview of the channel structure. This is followed by a detailed discussion of the operation of the monitor and Command/Indicate (C/I) channels, plus the activation/deactivation procedure for the IOM-2 bus. Subsequent sections provide examples of terminal, NT1, and line-card applications. The final section of the document provides a detailed description of the physical I/O and clock pins, DC characteristics, and AC signal timing.

The IOM-2 Bus

The IOM-2 bus provides a symmetrical full-duplex communication link, containing user data, control/programming, and status channels. Both the line-card and terminal portions of the IOM-2 standard utilize the same basic frame and clocking structure, but differ in the number and usage of the individual channels. The various channels are time-multiplexed over a four-wire serial interface. Data is clocked by a data clock (DCL) that operates at twice the data rate. Frames are delimited by an 8-kHz frame synchronization clock (FSC). Data is carried over data upstream (DU) and data downstream (DD) signals. Three additional signals are specified in the terminal mode to facilitate connecting components that do not directly support IOM-2. These are a 1X-bit rate clock (BCL), and two serial data strobes that identify the location of the B channels (SDS1 and SDS2).

LINE-CARD MODE

The line-card version of IOM-2 provides a connection path between line transceivers (ISDN) and codecs (analog), and the line-card controller; the line-card controller provides the connection to the switch backbone. The IOM-2 bus time multiplexes data, control, and status information for up to eight ISDN transceivers or up to 16 codec/filters over a single full-duplex interface. Figure 2-1 shows the block diagram of a typical ISDN or analog line card.

By providing data, control, and status information over a serial channel, the IOM-2 bus eliminates the need to have a microprocessor interface on the transceiver or codec. This reduces pin count and simplifies line-card layout, thus reducing cost.

Information is multiplexed into frames, which are transmitted at an 8-kHz rate. The frames are subdivided into from one to eight sub-frames, with one sub-frame being dedicated to each transceiver or pair of codecs. The sub-frames provide channels for data, programming, and status information for a single transceiver or a codec pair.

Figure 2-1 Typical Line-Card Configuration

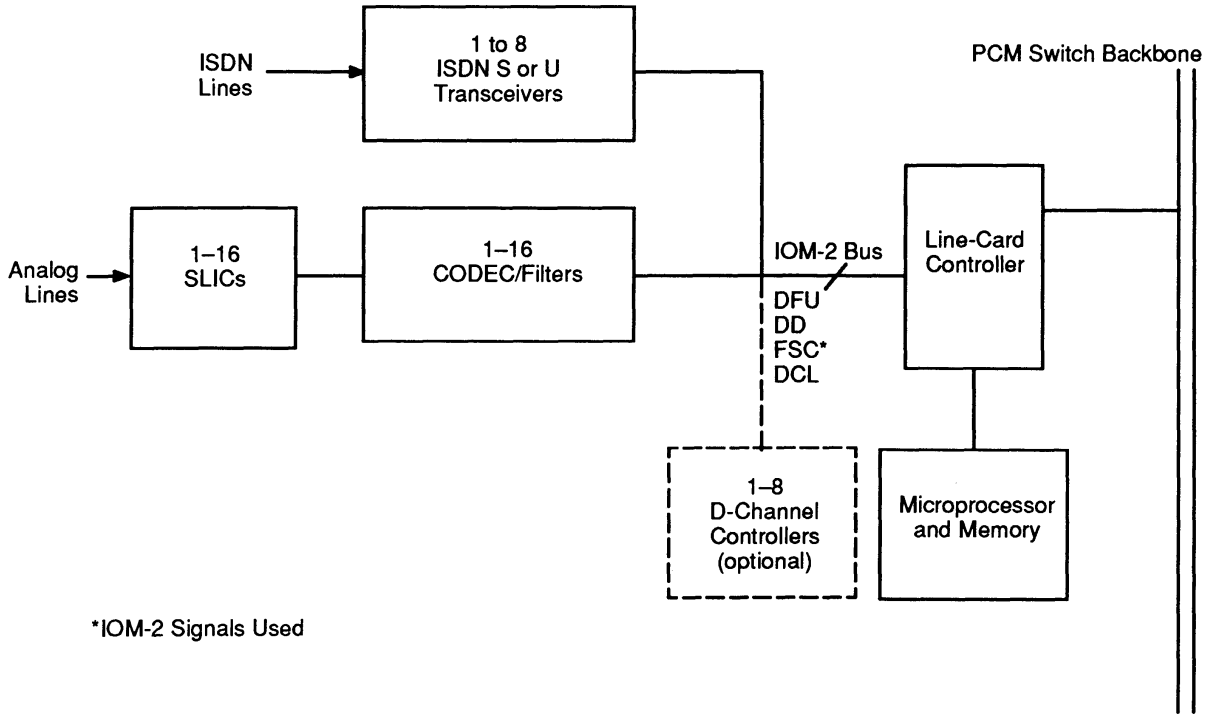
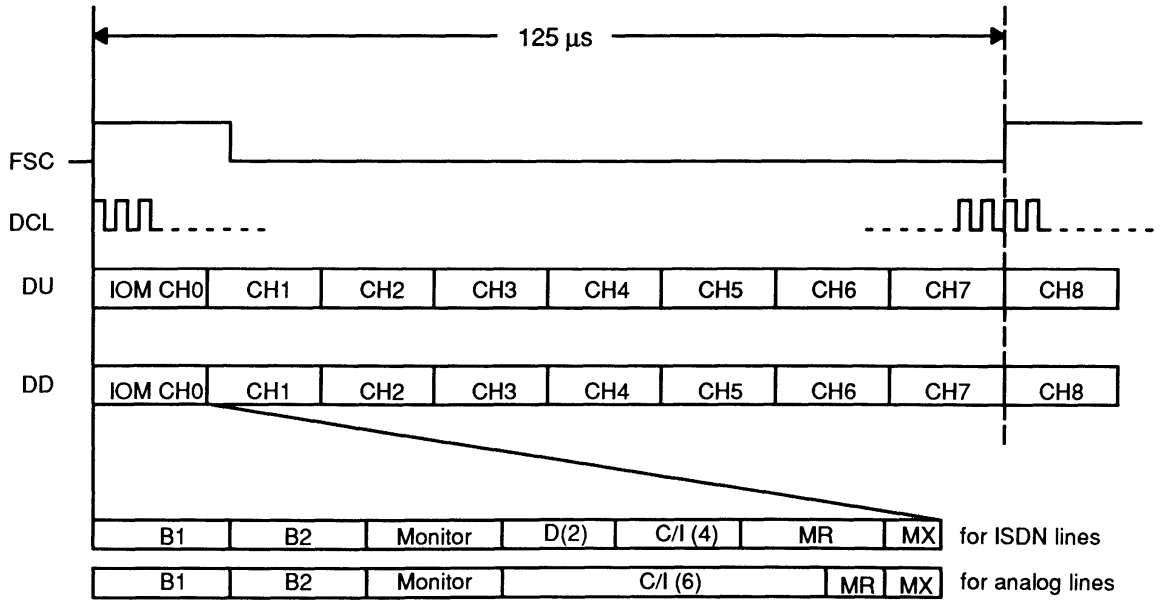


Figure 2-2 IOM-2 Line-Card Mode Frame Structure (DU and DD Shown for DCL = 4.096 MHz)



TERMINAL MODE

The terminal version of IOM-2 is a variation of the line-card bus, designed for ISDN terminal and NT1 applications, and serves four functions:

1. Connection of voice/data modules to a Layer 1 device (transceiver). Provisions are included for the connection of devices that do not have an IOM-2 interface.
2. Programming and control of devices that do not have a microprocessor interface, for example, a codec or a U-Interface transceiver.
3. Inter-chip communications between devices on the bus, for example, a codec to a speech encryption device.
4. Connection of multiple Data Link Controllers (DLCs) to the D channel, including access arbitration.

Figure 2-3 shows a block diagram of the IOM-2 terminal configuration.

TERMINAL MODE FRAME STRUCTURE

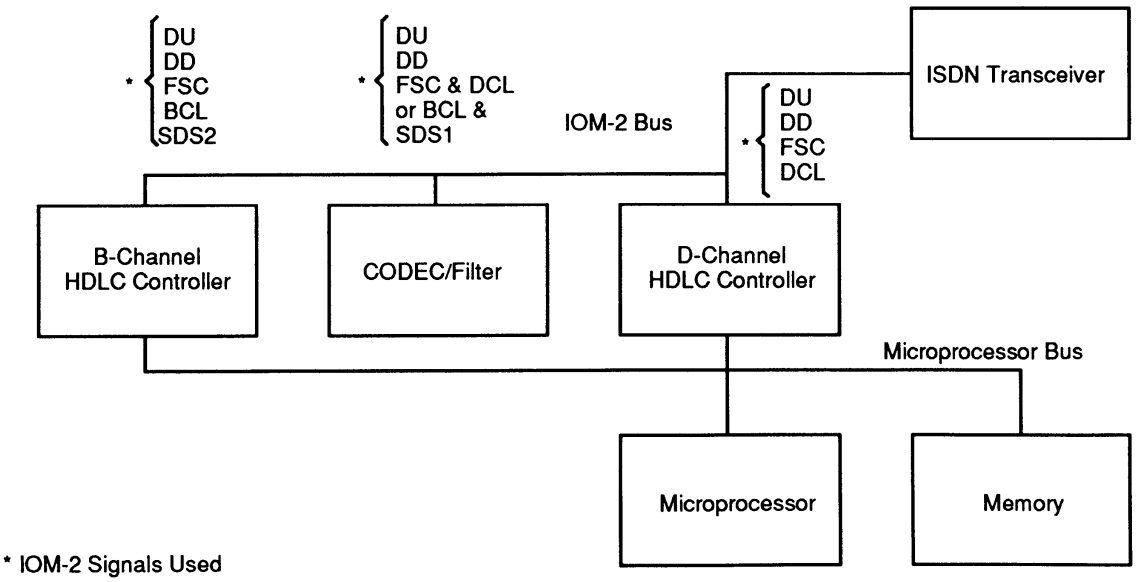
The IOM-2 terminal version consists of three sub-frames, each containing 32 bits. This 12-byte frame is repeated at 8 kHz, giving an aggregate data rate of 768 kb/s. The frame structure is shown in Figure 2-4.

Sub-Frame Utilization

The IOM-2 terminal mode frame is divided into three sub-frames of 4 bytes each. The first sub-frame is dedicated to controlling the Layer 1 transceiver (monitor and C/I channels) and passing user data (B and D channels) to the Layer 1 transceiver (or between two Layer 1 transceivers in the case of a repeater or NT1). This is evident as only the first sub-frame contains B and D channels. The monitor and C/I channels of the first sub-frame provide communications between a controlling device and the Layer 1 transceiver, or between two Layer 1 transceivers.

The second and third sub-frames are used for communication between a controlling device and devices other than the Layer 1 transceiver (monitor and C/I channels), or

Figure 2-3 Typical Terminal Configuration



between two user data processing devices (IC channels). The C/I channel of the third sub-frame is used for TIC bus applications. The TIC bus is described below.

Figure 2-5 shows an example of the logical routing of the sub-channels between components on the IOM-2 bus.

Figure 2-4 IOM-2 Terminal Mode Frame Structure

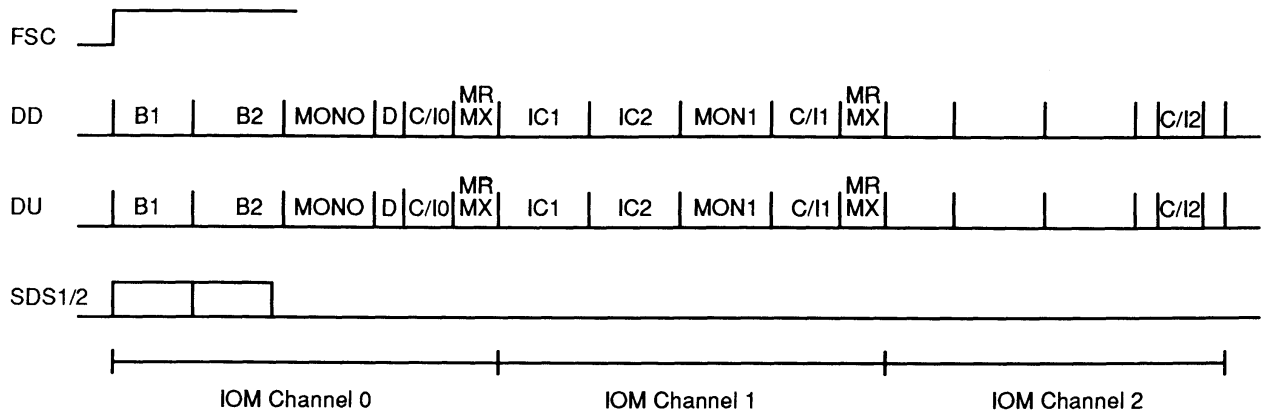
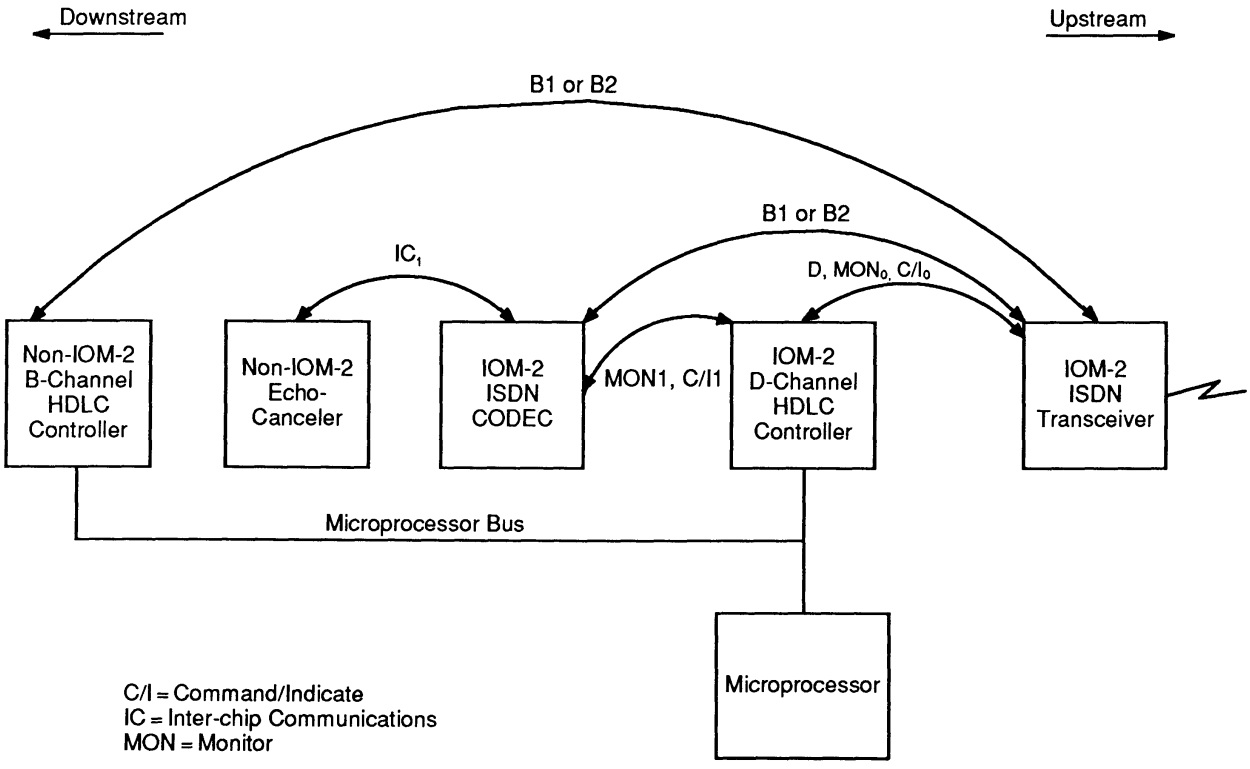


Figure 2-5 Example IOM-2 Channel Usage—Terminal Mode



Typical Channel Routing

As seen in Figure 2-4, the 12-byte frame contains the following channels:

B Channels

The B1 and B2 provide two clear 64-kb/s user data channels to/from the network.

Monitor Channels

There are two programming channels, Monitors 0 and 1. Each channel has an associated pair of MX and MR handshake bits that control data flow.

D Channel

The 16-kb/s D channel provides a connection between the Layer 2 and Layer 1 components.

Command/Indicate Channels

Three Command/Indicate channels, C/I 0, C/I 1, and C/I 2 provide real-time status between devices connected via the IOM-2 bus.

Intercommunication Channels

Two intercommunication data channels, IC1 and IC2 provide 64-kb/s data paths between user devices.

TIC Bus

One D-channel access bus, TIC bus. The TIC function is implemented using 4 bits of the C/I 2 channel, and allows multiple Layer 2 devices to individually gain access to the D and C/I channels (located in the first sub-frame).

PIN DIRECTION REVERSAL

The data signals on the IOM-2 bus are defined as Data Upstream (DU) and Data Downstream (DD). In terminal mode, a device may be required to transmit both upstream and downstream, based on which channel is being transmitted at any one time. For example, the D-channel HDLC controller in Figure 2-5 is downstream of the line transceiver, but upstream of the codec/filter. As a result, the actual data pins of the integrated circuit need to be both inputs and outputs, changing direction based on which channel is being transmitted at the time. The line transceiver in Figure 2-5 is always the upstream component, and never reverses its pins. The codec/filter is the downstream device when transmitting on the B channel, but upstream when transmitting the IC channel. The echo canceler and B-channel HDLC controller are always downstream, and do not need to reverse their pins.

CHANNEL STRUCTURE

The IOM-2 frame structure comprises 32-bit sub-frames containing time-multiplexed D channels. In the case of the line-card mode, each sub-frame contains an identical set of B, monitor, C/I and, optionally, D channels. The D channel is not used in analog application. In this case, the C/I channel is expanded to 6 bits using the 2 bits normally allocated to the D channel. In terminal mode, each of the three sub-frames contains a different set of channels. The first sub-frame is identical to the structure of the ISDN line-card mode sub-frame. The second and third sub-frames do not contain B or D channels, but support the monitor, IC, and TIC channels.

B CHANNELS

The B1 and B2 channels are physically the first two 8-bit timeslots after the frame sync pulse. Each B channel carries 64 kb/s of user data (or digitized voice).

D CHANNEL

The D channel contains 2 bits per frame, providing a 16-kb/s channel for carrying ISDN D-channel data. In analog line-card applications of IOM-2, there is no D channel; the adjacent C/I channel is increased to 6 bits.

MONITOR CHANNEL (INCLUDING MX, MR)

The monitor channels provide an interface between the microprocessor, via the line card controller (line-card applications) or the IOM-2 bus master (terminal applications), and devices attached to the bus. This allows these devices to be designed without their own microprocessor interface. Each channel consists of 8 bits of data and two associated handshake bits, MX and MR (monitor transmit and receive). The handshake procedure is described in the Monitor Channel Operation section.

COMMAND/INDICATE CHANNEL

The Command/Indicate channel (C/I) carries real-time status information between either a line transceiver or codec/filter and the line-card controller, or between the bus master and a line transceiver or a peripheral device on the terminal bus. In line-card applications, a C/I channel is 4 bits wide for ISDN applications and 6 bits wide for non-ISDN applications. In terminal applications, the C/I channel in the first and third sub-frames consists of 4 bits. In the second sub-frame, the C/I channel is 6 bits wide (bits 2–7 of the last octet).

Status information transmitted over the C/I channel is "static" in the sense that a 4- or 6-bit word is repeatedly transmitted, every frame, as long as the status condition that it indicates is valid. In general, the receiver monitors the C/I channel for changes in status. The definition and usage of the 4- and 6-bit C/I codes is described in the C/I Channel Operation section.

INTER-CHIP COMMUNICATION CHANNEL

The Inter-chip Communication channels, or IC channels, exist only in the terminal version of IOM-2, and provide 64-kb/s communications paths between devices other than the Layer 1 transceiver (data to and from the Layer 1 transceiver is transferred over the B channels).

TIC CHANNEL

The Terminal IC (TIC) bus is defined as the capability of connecting more than one device to the D and C/I channels in the first sub-frame (terminal mode only). Bus access and collision resolution is supported by the C/I channel in the third sub-frame. Support of the TIC capability is optional, based on system requirements. Its operation is described in the TIC Channel Access section.

CHAPTER 3

MONITOR CHANNEL OPERATION

HANDSHAKE PROCEDURE

The monitor channel is full duplex and operates on a pseudo-asynchronous basis, that is, while data transfers on the bus take place synchronized to frame sync, the flow of data is controlled by a handshake procedure using the MX and MR bits. For example: data is placed onto the monitor channel and the MX bit is activated. This data will be transmitted repeatedly (once per 8-kHz frame) until the transfer is acknowledged via the MR bit. Thus, the data rate is not 8K bytes per second.

Figure 3-1 shows the flow of events and Figure 3-2 shows the timing.

Idle

The MX and MR pair being held inactive for two or more frames constitutes the channel being idle in that direction.

Start of Transmission

The first byte of data is placed on the bus and MX is activated (Low). MX remains active, and the data remains valid until an inactive-to-active transition of MR is received, indicating that the receiver has read the data off the bus.

Subsequent transmission (general case, Figure 3-2a)—Remaining bytes of the message are transmitted as follows: the next byte is placed on the bus after the inactive to active transmission of MR_X—as early as the next frame (there is no limit to the maximum number of frames). At the time that the second byte is transmitted, MX is returned inactive for one frame time (MX inactive for more than one frame time indicates an End of Message). In response to MX going active, MR will be deactivated for one frame time (the MX inactive to MR inactive delay can be any number of frame times). This procedure is repeated for each additional byte.

Maximum speed case, Figure 3-2c—The transmitter can be designed for a higher data throughput than is provided by the general case described above. The transmitter can deactivate MX and transmit new data one frame time after MR is deactivated. In this way, the transmitter is anticipating that MR will be reactivated one frame time after it is deactivated, minimizing the delay between bytes. Note that MR being held inactive for two or more frame times indicates an abort is being signaled by the receiver.

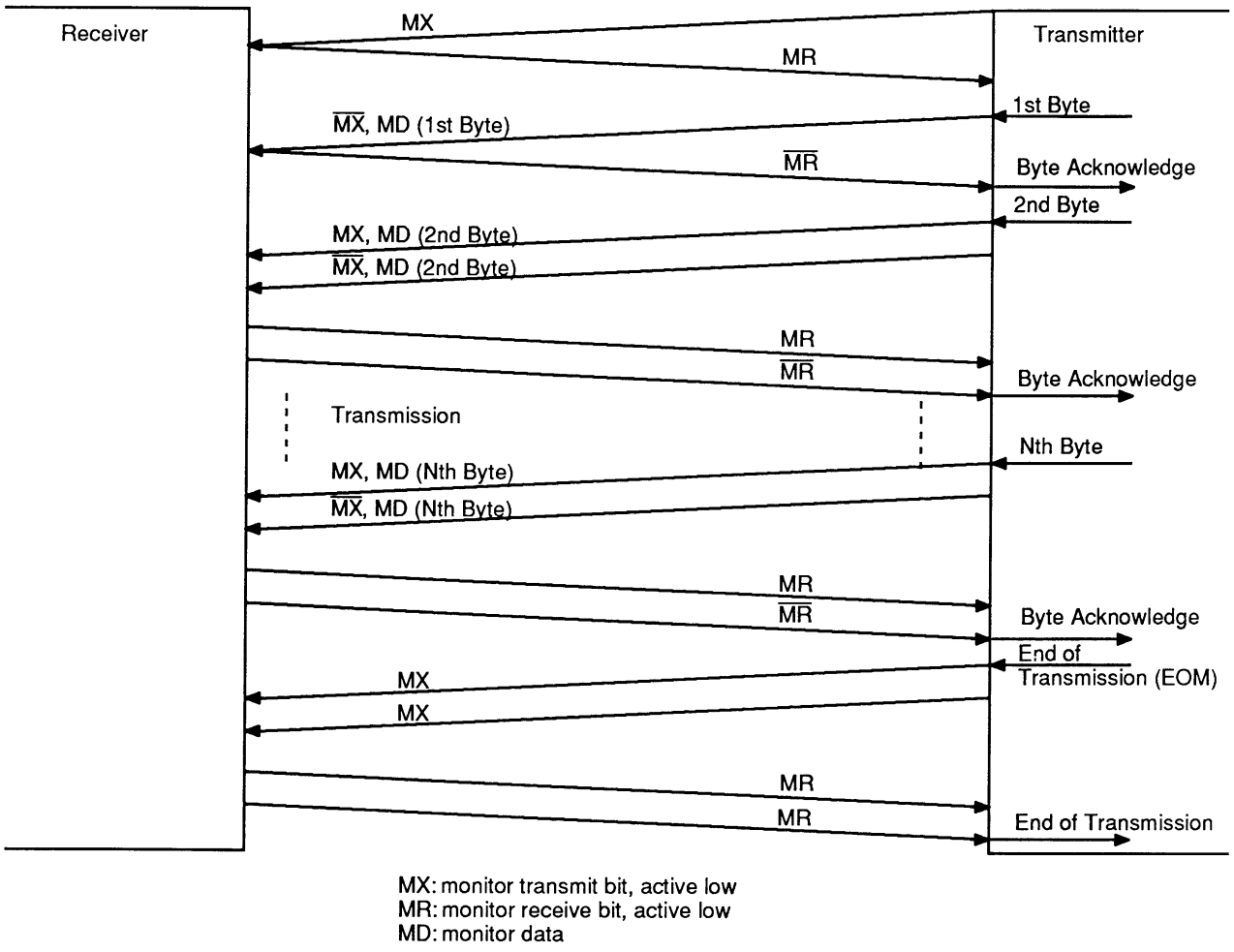
First Byte Reception

At the time the receiver sees the first byte, indicated by the inactive-to-active transition of MX, MR is by definition inactive. In response to the activation of MX, the data is read off of the bus and MR is activated. MR remains active until the next byte is received or an end of message is detected (MX held inactive for two or more frame times).

Subsequent Reception

Data is received from the bus on each falling edge of MX, and a monitor channel receive data available interrupt is generated. Note that the data may actually be valid at the time that MX went inactive, one frame time prior to going active. MR is deactivated after the data is read and reactivated one frame time later. The transmitter will

Figure 3-1 Monitor Handshake Procedure



MX: monitor transmit bit, active low
MR: monitor receive bit, active low
MD: monitor data

detect MR going inactive and anticipate its reactivation one frame time later. The transmission of the next data byte will begin at the same time that MR is going active.

The reception of data is terminated by the receipt of an end-of-transmission indication (MX remaining inactive for two or more frame times).

End Of Transmission (EOM)

The transmitter sends an EOM, normally after the last byte of data has been transmitted, by simply not reactivating MX after deactivating it in response to MR going inactive.

Abort

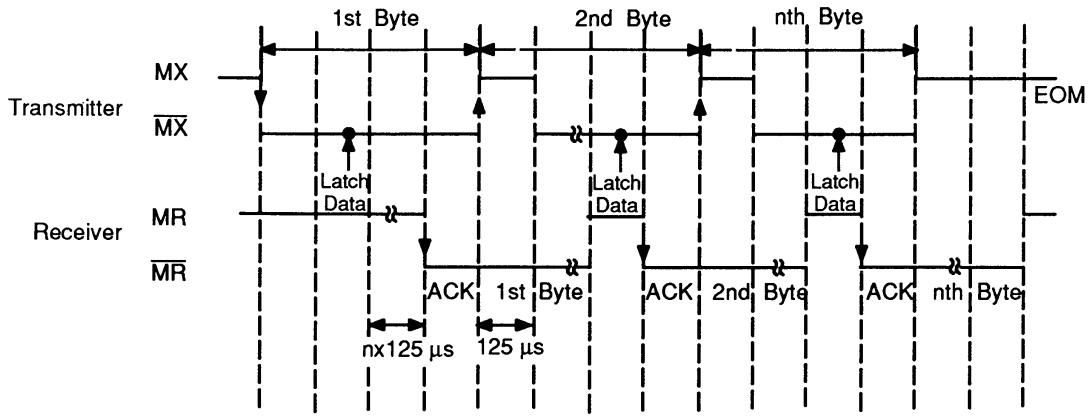
The abort is a signal from the receiver to the transmitter indicating that data has been missed. It is not an abort in the classical sense, which is an indication from the transmitter that the current message should be ignored. The receiver indicates an abort by holding MR inactive for two or more frames in response to MX going active.

Flow Control

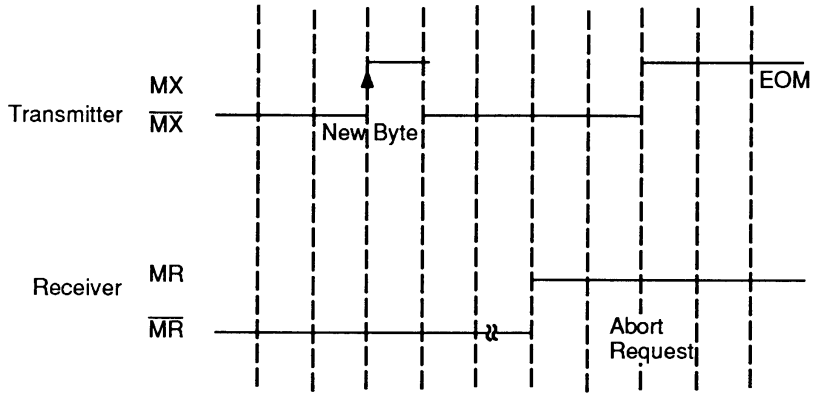
The receiver can hold off the transmitter by keeping MR active until the receiver is ready for the next byte. The transmitter will not start the next transmission cycle until MR goes inactive.

Figure 3-2 Monitor Handshake Timing

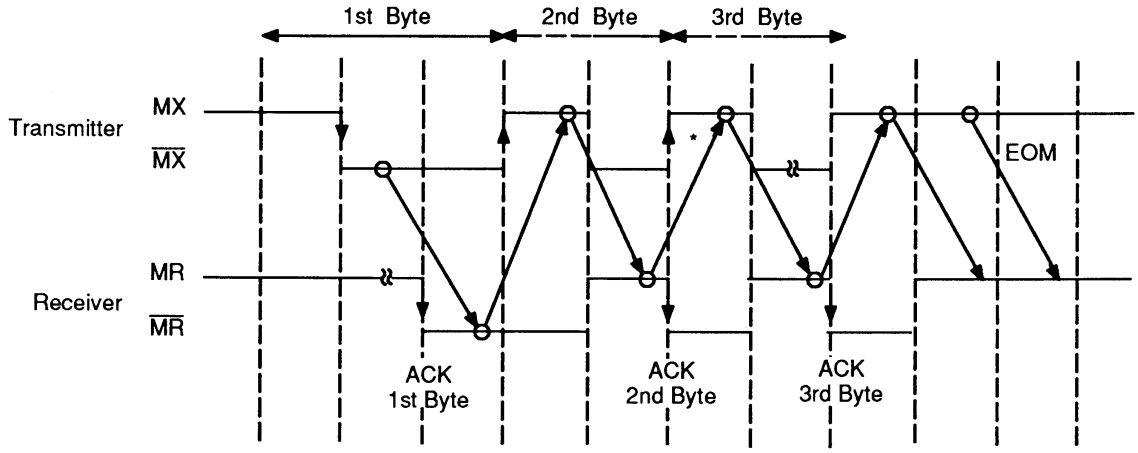
a. General Case



b. Abort Request from the Receiver



c. Maximum Speed



* For maximum speed the transmitter anticipates the falling edge of the receiver's acknowledgment.

MONITOR CHANNEL DATA STRUCTURES AND ADDRESSING

Message Type/Address Codes

The information transported across the monitor channel interface depends on the downstream devices connected to the IOM-2 bus. The first four bits (7–4) of the first byte of the monitor channel message contain the monitor channel address.

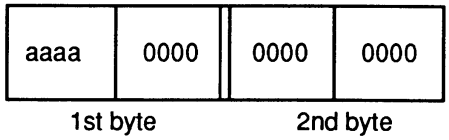
Code	Message Type/Address	
0000	12-bit 2B1Q U-interface Embedded Operations Channel (EOC)	
0001	S/T interface S1 maintenance channel	
0010	S/T interface S2 maintenance channel	
0011	S/T interface S3 maintenance channel	
0100	S/T interface S4 maintenance channel	
0101	S/T interface S5 maintenance channel	
0110	Reserved	(Example: IOM-2 terminal devices)
0111	Reserved	
1000	Local functions or analog line devices	
1001	Analog line device	(Example: IOM-2 terminal devices)
1010	Reserved	
1011	Reserved	
1100	Reserved	
1101	Reserved	
1110	Reserved	
1111	Reserved	

Examples

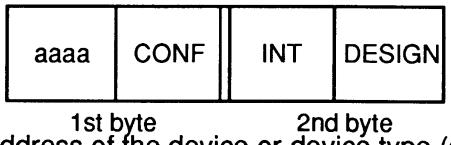
Addressing of ISDN devices on the line card is handled using the 1000 local functions code. Addressing of analog line codec/filters on the line card is handled using the 1000 (and 1001) analog line device codes.

Channel Identification Command

In order to identify different devices by software, an identification command is defined for all IOM-2 devices. A device requesting the identity of another device will transmit the following 2-byte code:



The responding device will transmit:



where aaaa is the address of the device or device type (see preceding section).

CONF: An optional 4-bit code indicating the specific hardware environment; this is primarily used for analog applications. A typical application of the CONF code is the differentiation of various types of line circuits that use the same codec/filter/SLIC hardware within the same system, for example, private circuits, DDI circuits, etc.

Codes are also reserved for addressing devices in an IOM-2 terminal; for example: 0111 for terminal adaptors and 101X for addressing codec/filters.

INT: Line interface type, 2 bits:
00 = U interface
01 = S/T interface
10 = Analog line
11 = Reserved

Design: The 6-bit design field is used to differentiate between different implementations of the same function.
Codes 0–7 are reserved by AMD/Siemens
Codes 8–15 are reserved by SGS/Thomson/National
Codes 16–19 are reserved by Plessey
Codes 20–23 are reserved by GEC/MEDL
Codes 56–63 are available for use in custom devices that contain an IOM-2 interface, and will be used within a single company's products (example: ASICs).

CHAPTER 4

C/I CHANNEL OPERATION

The C/I channel is used to communicate real time status information and maintenance commands, such as loopback requests, link activation/deactivation procedures, and switch hook/ground key detection (voice channels). Data on the C/I channel is continuously transmitted in each frame until new data is to be sent. In this way, the C/I channel can be thought of as a set of static status lines that only change when the status changes.

Data Integrity

Where data integrity is a concern, a change in C/I channel data may be considered valid if it has been received in two consecutive frames.

Multiple Layer 1 Links

In the case where multiple Layer 1 devices are connected along a line, such as a repeater or NT1 function, each device will interpret the C/I channel commands, taking the action required by the command, or passing the command upstream or downstream.

ISDN APPLICATIONS

The usage of the C/I channel in the IOM-2 line-card mode (ISDN) and in the first sub–frame of the terminal mode is identical. The definition of the codes used over these two channels is described in the C/I code section below.

Terminal Mode Channel Utilization

The C/I channel in the first sub-frame is used for communication between a controlling device and the Layer 1 transceiver in terminal devices, or between two Layer 1 devices in repeaters and NT1 devices. The second sub-frame C/I channel is 6 bits wide and is used for communication between two non-Layer 1 devices. The 64 possible codes for this C/I channel are not defined by the IOM-2 standard and are application specific. The third sub-frame C/I channel is used for the TIC bus.

COMMAND/INDICATION CODES (C/I) CODES

The following is a description of the different commands and indications that are used over the IOM-2 interface for signaling and control in ISDN systems.

Downstream (DD)

DR Deactivation Request. Must be maintained at least 0.5 ms to ensure that the downstream device reaches its final state before its indication is sensed.

DC Deactivation Confirmation. Informs the downstream device that the upstream device has been deactivated. Both devices are ready to receive wake signals.

PU Power Up. Optional response to a request from the downstream device asking for a clock to activate the IOM-2 interface.

ARD Activation Request Downstream. The upstream device is synchronous. The ARD can be one of the following:

AR Activation Request
ARL Activation Request Local test loop
AR2 Activation Request test loop 2 (NT1)
AR4 Activation Request test loop 4 (RPT)

UAR U only Activation Request

AID Activation Indication Downstream. The data is now switched through transparently. The AID can be one of the following:

AI Activation Indication
AIL Activation Indication Local loop
AI2 Activation Indication loop 2 (NT1)

RES Reset. Software reset.

TM1 Test Mode 1. Special test mode for making line measurements.

TM2 Test Mode 2. Special test mode for making line measurements.

Upstream (DU)

TIM Timing requested for activating IOM-2 interface.

DI Deactivation Indication. Downstream devices are all deactivated.

ARU Activation Request Upstream. Wake signal received or wake procedure fulfilled. The ARU can be one of the following:

AR Activation Request
ARL Activation Request Local test loop
AR8 Activation Request priority 1
AR10 Activation Request priority 2

Note: AR10 is only for S/T interface terminals.

UAI U Activation Indication. U transmission line is synchronous.

AI Activation Indication. Downstream sections are all synchronous.

RES Reset. Software reset.

TM1 Test Mode 1. Special test mode for making line measurements.

TM2 Test Mode 2. Special test mode for making line measurements.

Transitions

Transitions are initiated by well-defined signals (infos) on transmission lines or by Layer 2 events.

AR–U Activation Request Upstream. Initiated from TE.

AR–D Activation Request Downstream. Initiated from the exchange.

SY–U Synchronous Upstream. The downstream device on the IOM-2 interface has been synchronized.

SY–D Synchronous Downstream. The upstream device on the IOM-2 interface has been synchronized.

SY Synchronous. The last device downstream has been synchronized. The reception of this message at the exchange indicates that the entire transmission line has been synchronized.

CT–D Connection Through Downstream. Command for transparent switching of data.

DR–D Deactivation Request Downstream. Initiated from the exchange.

DI–U Deactivation Indication Upstream. The downstream line is deactivated.

Maintenance Information

Transmission devices are able to send error conditions or unsolicited maintenance information through the C/I channel provided they are in an active state. When the error has been corrected (error recovery) or the maintenance information has been transferred, the interface returns to the state it was in before the error occurred.

Exceptions:

- Deactivation
- Additional error messages postpone return to original state.

List of Error Messages:

RSY Resynchronization. Loss of synchronization.

SLIP Slip detected in framing. A phase difference may appear at the interface between the public exchange and a PABX. To account for this the master (upstream) device indicates with the message "SLIP" that one frame (18 data bits) was repeated or ignored (data buffer overflow or underflow).

Unsolicited maintenance information may be conveyed by using the free C/I codes (see Table 4-1). Detailed functions are to be defined in the component specifications.

Table 4-1 can be used as a quick reference for all of the possible C/I code values along with the abbreviations for their respective commands and indications. A glossary of these abbreviations is given in Table 4-2.

Table 4-1 C/I Codes

Code	TE		NT1		RPT		LT	
bits 4:1	DD	DU	DD	DU	DD	DU	DD	DU
0000	DR	TIM	DR	TIM	DR	TIM	DR	TIM
0001	RES	RES	RES	RES	RES	RES	RES	RES
0010	—	TM2	TM2	TM2	TM2	TM2	TM2	—
0011	—	TM1	TM1	TM1	TM1	TM1	TM1	—
0010	RSY	—	RSY	RSY	RSY	RSY	—	RSY
0101	—	—	—	—	—	—	—	—
0110	—	—	—	—	—	—	—	—
0111	PU	—	PU	—	UAR	UAI	UAR	UAI
1000	AR	AR8	AR	AR	AR	AR	AR	AR
1001	—	AR10	—	—	AR2	—	AR2	—
1010	ARL	ARL	ARL	ARL	ARL	—	ARL	—
1011	—	—	—	—	—	—	AR4	—
1100	AI8	—	AI	AI	AI	AI	AI	AI
1101	AI10	—	—	—	AI2	—	—	—
1110	AIL	—	AIL	—	AIL	—	—	—
1111	DC	DI	DC	DI	DC	DI	DC	DI

Undefined codes indicated by "—"
DD: C/I code downstream
DU: C/I code upstream

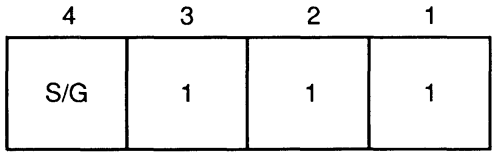
Table 4-2 List of Commands and Indications

Command/Indication	Abbreviation
Activation Indication	AI
Activation Indication priority 1	AI8
Activation Indication priority 2	AI10
Activation Indication test loop 2	AI2
Activation Indication local test loop	AIL
Activation Request	AR
Activation Request priority 1	AR8
Activation Request priority 2	AR10
Activation Request test loop 2	AR2
Activation Request local test loop	ARL
Activation Request test loop 4	AR4
Deactivation Confirmation	DC
Deactivation Indication	DI
Deactivation Request	DR
Power Up	PU
Reset	RES
Resynchronization (loss of framing)	RSY
Slip detected in framing	SLIP
Timing required (to activate IOM-2)	TIM
Test Mode 1	TM1
Test Mode 2	TM2
U only Activation Indication	UAI
U only Activation Request	UAR

TIC CHANNEL ACCESS

In the downstream direction, the C/I channel in the third sub-frame is used for D and C/I0 channel access control in S/T interface terminals.

The availability of the S/T interface D channel is indicated in bit 4 of the downstream C/I channel.

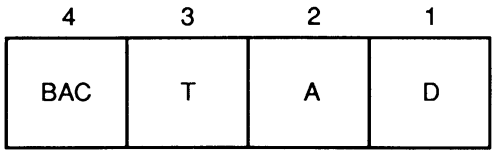


High: Stop
Low: Go

The stop/go bit is checked by the D-channel protocol controller to determine if it has access to the D channel. If it does, it can start transmission of an HDLC frame. If it does not have access, it must abort the transmission.

In the upstream direction, the C/I channel in the third sub-frame is used for the TIC channel access procedure, enabling the connection of several Layer 2 D-channel protocol controllers to the IOM-2 interface.

The C/I Channel 2 upstream has the following format:



BAC: Bus Access Bit
TAD: TIC-Bus Address

An access request may either be generated by software (microprocessor access to C/I Channel 0) or by the D-channel protocol controller itself (transmission of an HDLC frame). In the case of an access request, the D-channel protocol controller checks the BAC bit for the status "bus free" (BAC = 1). If the bus is free, the D-channel protocol controller starts transmitting its individual TIC bus address. If an erroneous address is detected, the procedure is terminated immediately. If the complete TIC bus address can be transmitted without error, the D channel and C/I Channel 0 are immediately occupied; during the subsequent frames the bus is identified as occupied (BAC = 0) until the access request is withdrawn. After a successful bus access, the D-channel protocol controller is set into a lower priority class, that is, a new bus access cannot be performed until the status "bus free" (BAC = 1) is indicated in two successive frames.

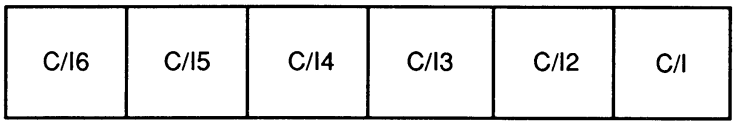
If none of the D-channel protocol controllers connected to the IOM-2 interface request access to the D and C/I channels, the TIC Bus Address 7 will be present. The device with this address will therefore have access, by default, to the D and C/I channels.

ANALOG APPLICATIONS

In analog line-card applications the C/I channel is 6 bits wide. The definition of these bits is dependent on the direction of the channel, that is, upstream or downstream.

The C/I Channel DD (Downstream)

The Downstream C/I channel takes the following format:



New incoming data over the C/I channel has to be stable for two consecutive frames before it is acted upon. If the incoming C/I data does not match the previous validated C/I data as stored in the C/I input register, then the codec/filter can be designed to follow either of the following two options, either being compatible with the IOM-2 definition.

Minimum Data Security (Option 1)

A flag is set to indicate that a change has been detected. If the C/I data in the following frame still does not correspond to the data in the C/I input register, then the new data is loaded into the C/I input register, and the flag is reset. If the C/I data in the following frame does correspond to the pattern already set in the C/I input register, then the flag is reset and the contents of the C/I input register remain unchanged.

Maximum Data Security (Option 2)

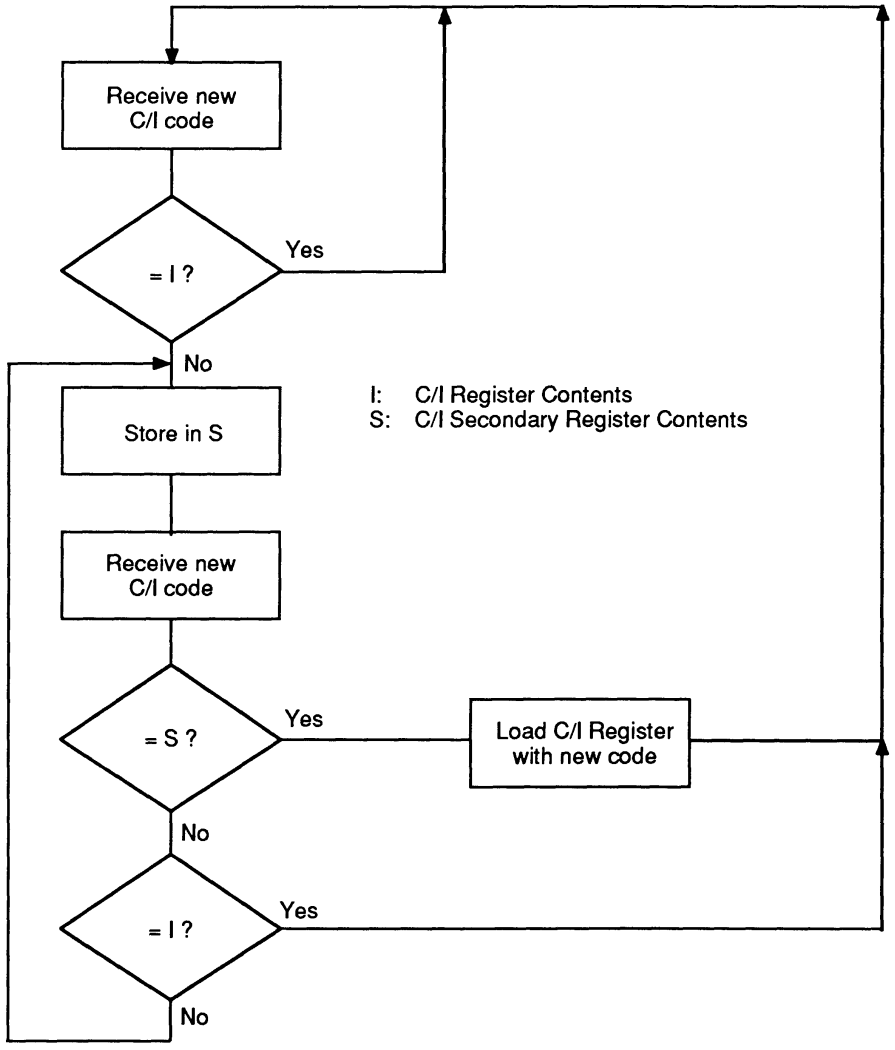
The received C/I bits are loaded into a secondary C/I register and a flag is set. If incoming data in the following frame corresponds to the pattern in the secondary C/I register, then the new pattern is loaded into the C/I input register, and the flag is reset.

If the new data does not correspond to the pattern in the secondary C/I register but does correspond with the data in the C/I input register, then the flag is reset; otherwise, the new data is loaded into the secondary C/I register and the flag remains set.

This option is shown in Figure 4-1.

The second (maximum security) option is the preferred option.

Figure 4-1 Security Procedure for C/I Downstream Byte



The C/I Channel on DU (Upstream)

C/I6	C/I5	C/I4	C/I3	C/I2	C/I1

USING THE C/I CHANNEL FOR MAINTENANCE

Figures 4-2, 4-4, and 4-6 illustrate the handling of error messages (for example, loss of synchronization). This information can be used by the appropriate software for error recovery. After error recovery, the IOM-2 interface returns to the original state. Refer to the "C/I codes" for explanations of the different messages.

Unsolicited maintenance information (UMI) may be conveyed to the exchange using the C/I channel. If this information is transferred in the U interface's maintenance channel, the activated state will be maintained (Figures 4-3, 4-5, and 4-7).

Switching of test loops is done with different activation commands (See Table 4-2). Switching between different test loops and the transparently activated state may be done arbitrarily by use of the different commands (Figure 4-8).

Figure 4-2 **Handling of Error Conditions in the LT**

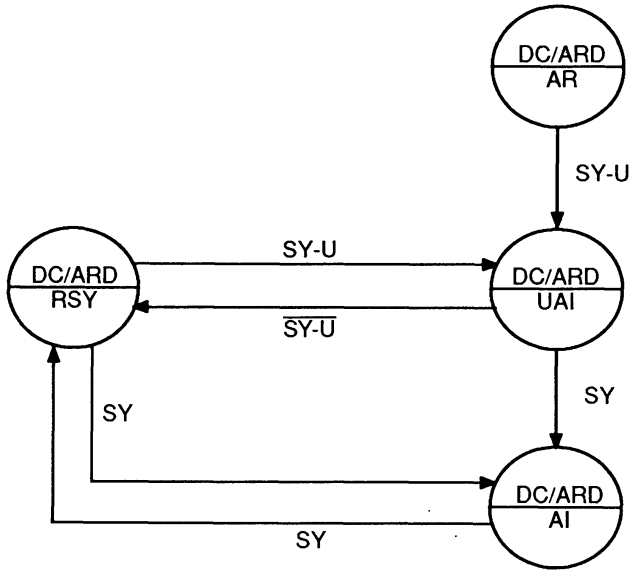


Figure 4-3 **Monitoring of Unsolicited Maintenance Information (UMI) in the LT**

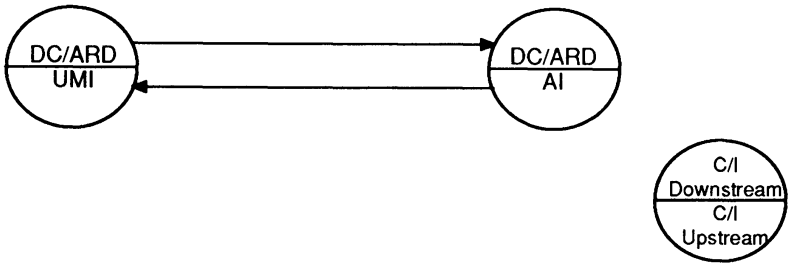


Figure 4-4 **Handling of Error Conditions in the TE**

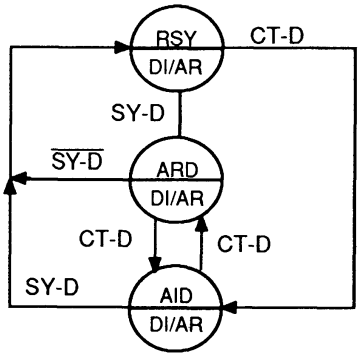


Figure 4-5 **Monitoring of Unsolicited Maintenance Information (UMI) in the TE**

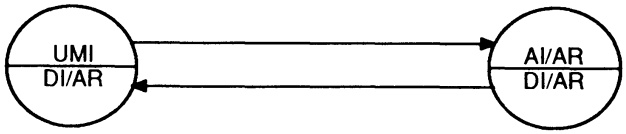
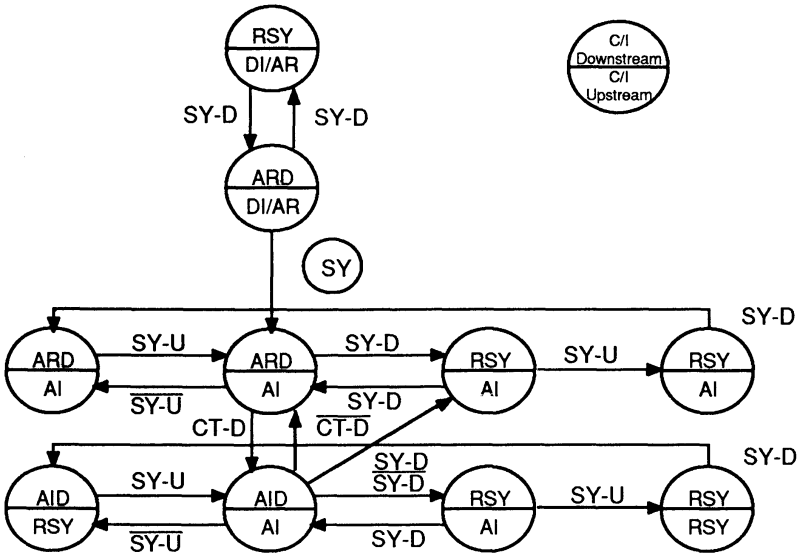


Figure 4-6 Handling of Error Conditions in NT and RPT



Note: Transition is dependent on synchronization procedure on the U interface.

Figure 4-7 Monitoring of Unsolicited Maintenance Information (UMI) in NT and RPT

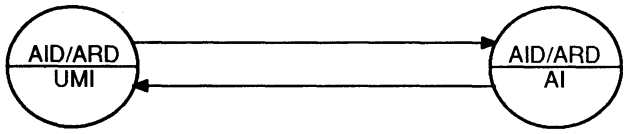
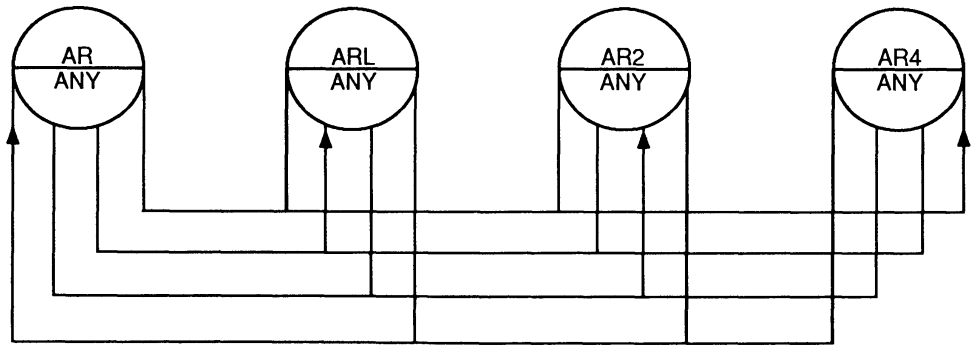


Figure 4-8 Commands for Switching Test Loops



CHAPTER 5

BUS ACTIVATION

The IOM-2 bus has an activation/deactivation capability. Activation and deactivation can be initiated from either the upstream or downstream component on the bus. When deactivated, DCL is held low and the data lines are held high. The activation/deactivation procedure is a combination of software handshakes via the C/I channel, and hardware indications via the clock and data lines.

Deactivation Request, Downstream To Upstream

There is currently no defined procedure for requesting deactivation from downstream.

Deactivation, Upstream To Downstream

The upstream unit can initiate deactivation via a series of software handshakes via the C/I channel. The upstream unit issues a deactivation request and waits for a deactivation indication from all downstream units. Once this is received, a deactivation confirmation is issued, followed by the stopping of DCL, BCL, and FSC, and the placing of the output pin in a high impedance state. After the clocks are stopped, the input pin is monitored for the presence of a timing request from the downstream unit (the input pin being pulled low).

Activation Request, Downstream To Upstream

The downstream unit can request that the clocks be restarted by pulling its data output line low (this is called a timing request). Once the clocks are restarted, the downstream unit requests activation by sending an activation request upstream over the C/I channel.

Activation, Upstream To Downstream

The upstream unit activates the bus by starting the clocks and following the C/I channel-based activation handshake procedure.

C/I CHANNEL ACTIVATION/DEACTIVATION HANDSHAKE PROCEDURES

Figure 5-1 illustrates the general activation/deactivation procedure between the terminal (TE) and the exchange (LT).

POWER DOWN (DEACTIVATION)

Subscriber lines for an ISDN Basic Access connection are activated on a call-by-call basis. For reasons of power conservation, each line is in a "power down" or deactivated state when not in use. All IOM-2 interfaces (except in the LT) are correspondingly deactivated during the idle state and must first be activated before the exchange of C/I information is possible.

In TE, NT, and RPT applications, the IOM-2 interface can be switched off in the inactive state, reducing power consumption to a minimum. In this deactivated state, the DCL clock line is low and the data lines are high.

The deactivation procedure is shown in Figure 5-2. After detecting the code DI (Deactivate Indication) from the downstream unit, the upstream unit responds by transmit-

Figure 5-1 **Example of Activation and Deactivation of U and S Interfaces**

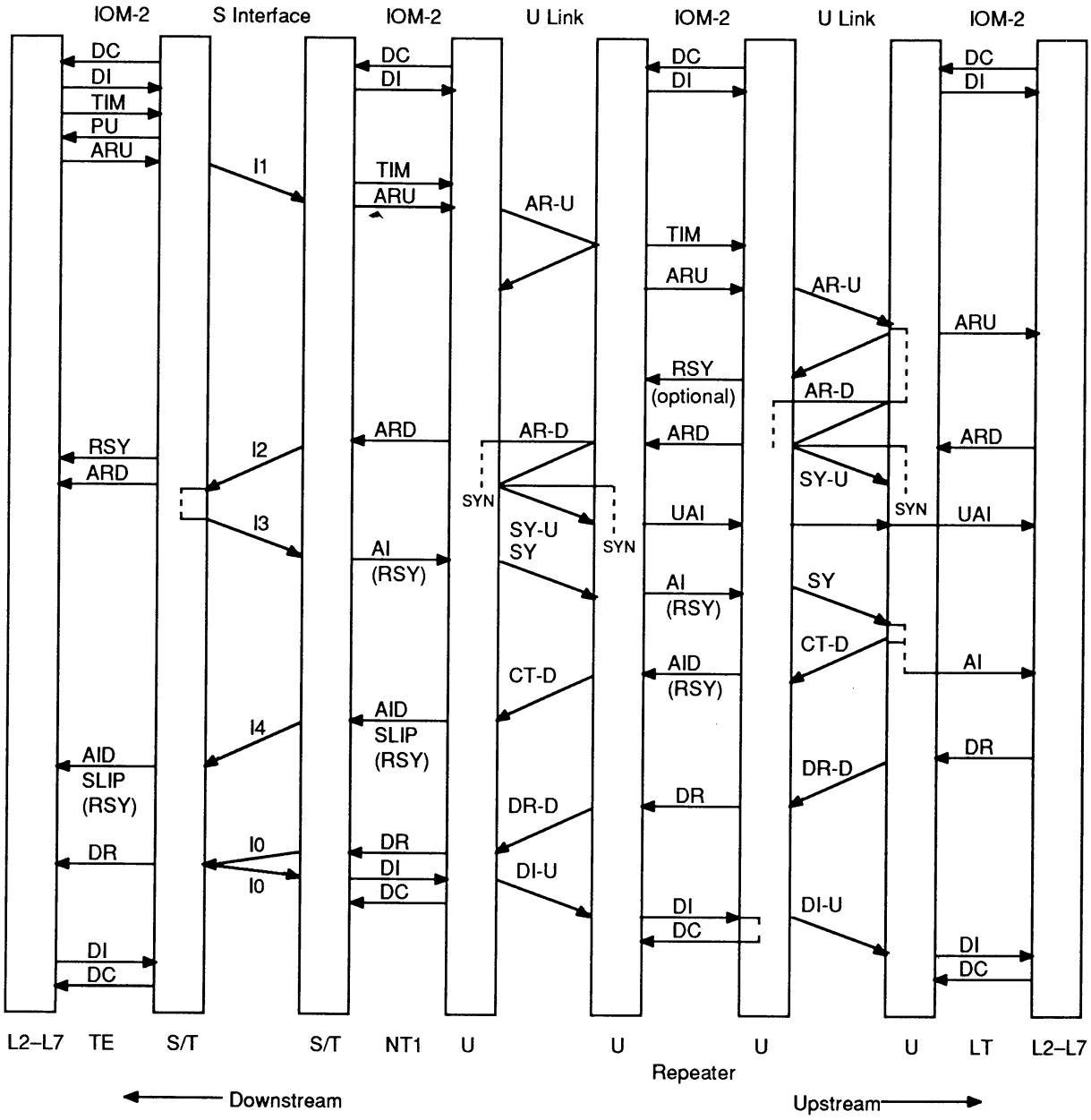
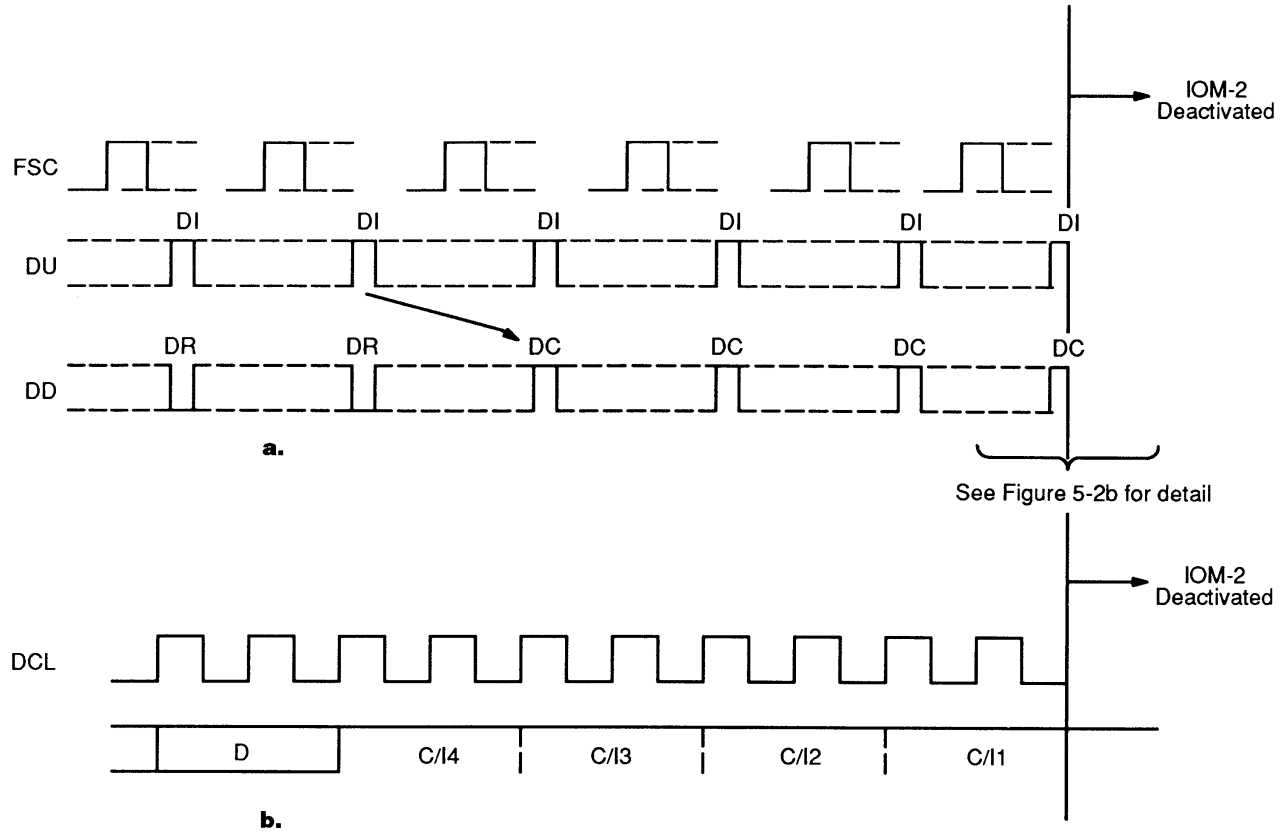


Figure 5-2 Deactivation of the IOM-2 Interface



ting DC (Deactivate Confirmation) during subsequent frames. The upstream unit stops sending timing signals after it has transmitted the last bit of the fourth consecutive DC command.

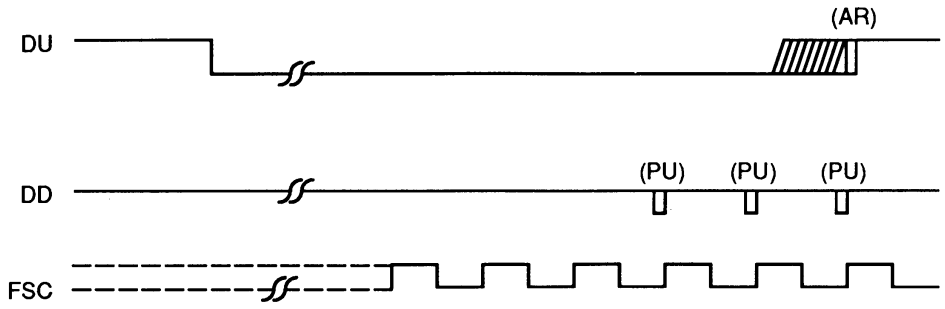
The clock pulses will be enabled again when the upstream unit recognizes a low level on DU (command Timing TIM = 0000) or when the upstream unit goes into the power-up state.

After the clocks have been enabled, this may be indicated by the PU code in the C/I channel. The downstream unit may then insert a valid code in the C/I channel. The continuous supply of timing signals by the upstream unit is ensured as long as there is no DI indication in the upstream C/I channel. If timing signals are no longer required and activation is not yet requested, the downstream unit may indicate this by sending DI.

Activation on the Line Initiated by TE

1. The processor writes the bit command code "Activation Request" (upstream: AR) in the C/I register of the Layer 2 device. This code is transmitted in the C/I channel of the IOM-2 interface towards a Layer 1 device that responds by sending a "wake" signal upstream on its transmission line. The Layer 1 device at the other end of the line section detects the wake signal and translates it into the 4-bit C/I code, to be sent further to the device connected to its IOM-2 interface. If this is again a Layer 1 device, it emits a wake signal upstream to the device at the other end of its transmission line. The same process is repeated until the wake signal reaches the line termination (LT).
2. The LT recognizes the wake signal and transmits it in the form of the C/I code to the Layer 2 device that in turn sends an interrupt request to its processor. Fur-

Figure 5-3 **Activation of the IOM-2 Interface**



Note: Duty cycle of FSC is not to scale (varies according to application).

ther, the LT, after a minimal delay following the reception of the wake signal, emits back a certain synchronization sequence downstream on the transmission line. This sequence will allow the downstream device closest to LT to synchronize itself. After the synchronization of the first device downstream has taken place, it proceeds by starting a handshake sequence with LT and simultaneously sends the command word "Activation Request Downstream" (ARD) on its IOM-2 interface downstream.

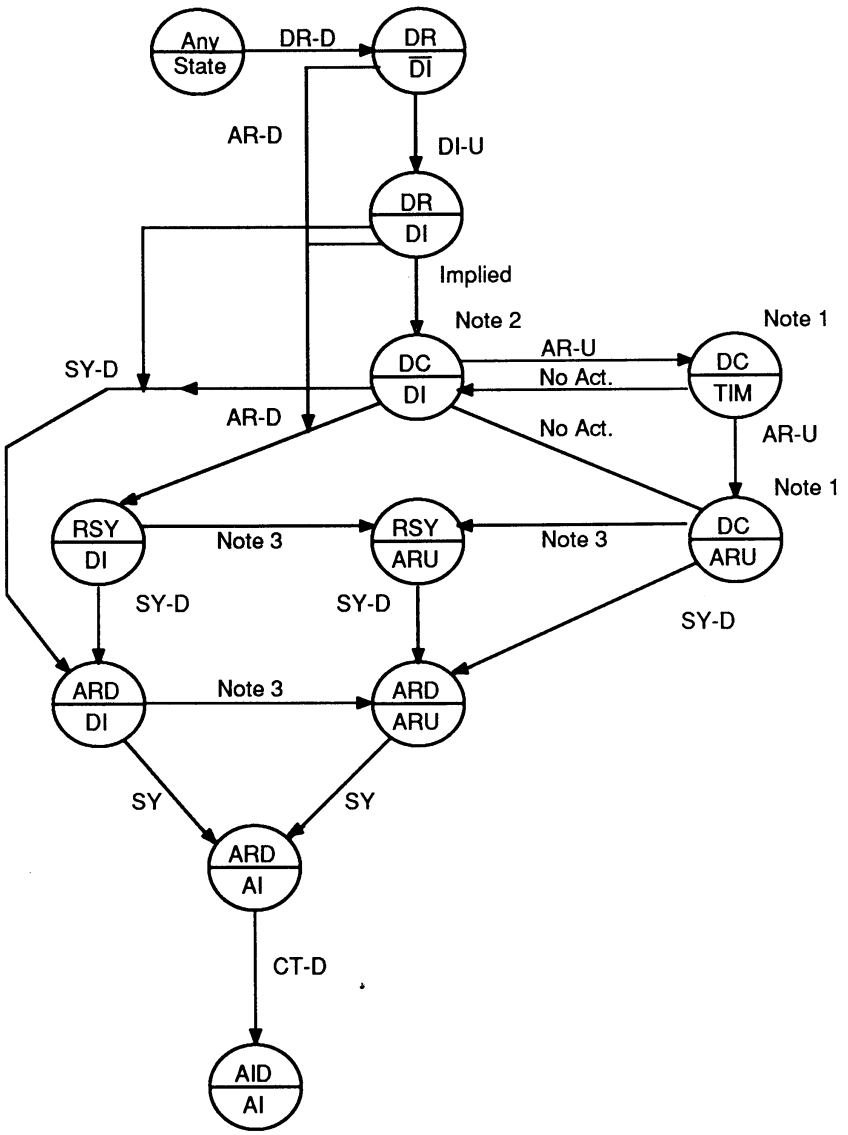
3. After the last transmission line section downstream has been synchronized, a response will be propagated upstream in the form of the message "Activation Indication" (AI).
4. Transparent data transmission starts as soon as the LT has received the AI message.

Activation of the Line Initiated by LT

1. The activation may be initiated at the exchange by the processor writing the command code for "Activation Request Downstream" (ARD) into the C/I register of the Layer 2 device. The code is then transmitted downstream over the IOM-2 interface in the C/I channel to the Layer 1 device. The Layer 1 device consequently sends a wake signal downstream on its transmission line section, with the result that both Layer 1 devices eventually become synchronized.
2. When the first line section downstream has been synchronized, the command ARD is sent on the next IOM-2 interface and consequently on the next transmission line section. This section will then be synchronized in the same manner.
3. When the last transmission line section at the TE becomes synchronized, this synchronization condition is eventually indicated by an AI message upstream in the LT.
4. On receiving AI message, transmission of transparent data can begin.

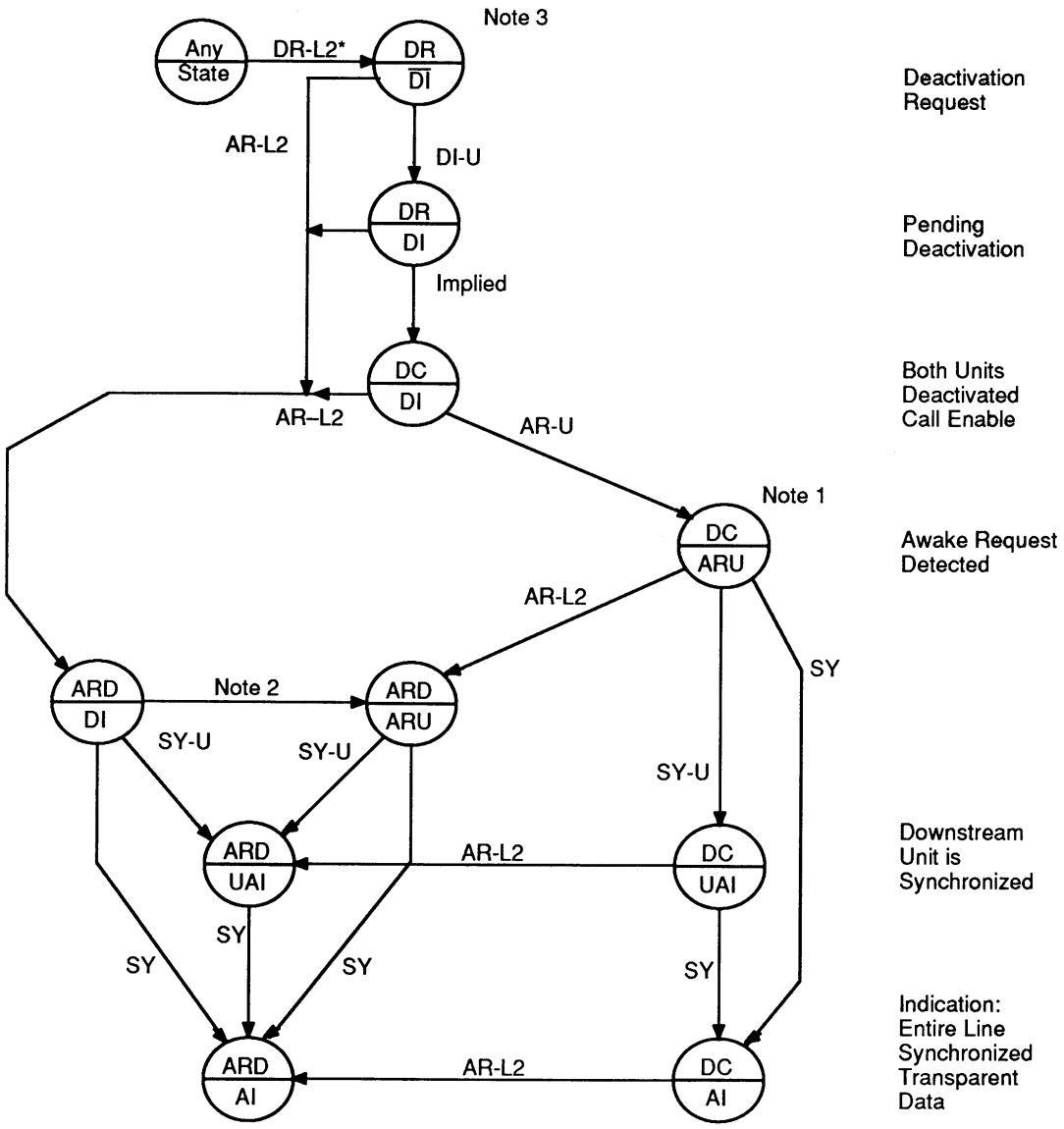
The dialog on the IOM-2 interface during the activation/deactivation procedure is described in the state diagrams illustrated on the following pages (Figures 5-4, 5-5, 5-6, and 5-7).

Figure 5-4 Activation/Deactivation Protocol for the IOM-2 Interface in the NT



Notes: 1. PU is allowed instead of DC.
2. In this state it is possible to switch the IOM interface to power down.
3. These transitions may be implemented for reasons of circuit simplification.

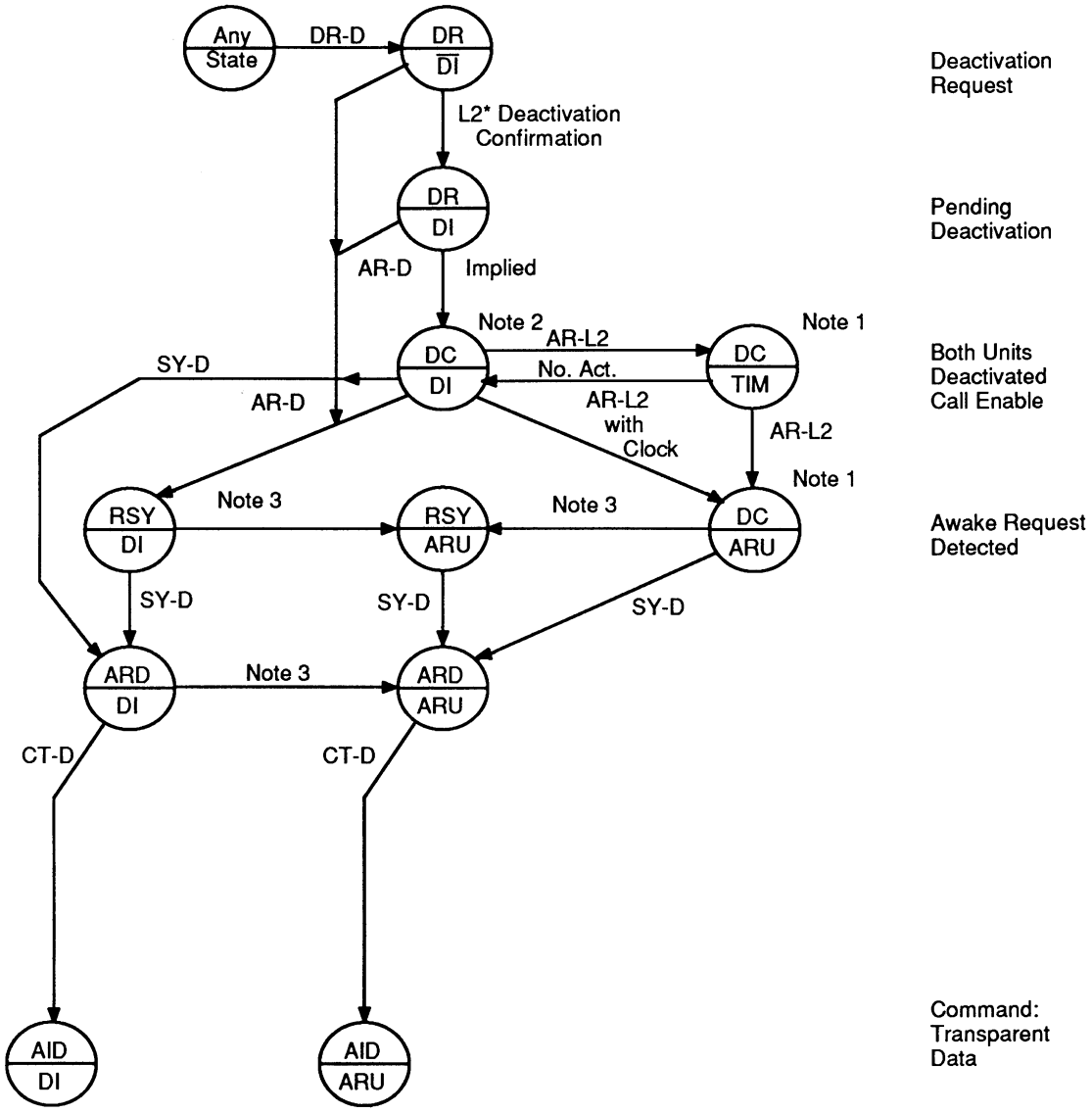
Figure 5-5 Activation/Deactivation Protocol for the IOM-2 Interface in the LT



* L2 = Layer 2

Notes: 1. PU is allowed instead of DC.
2. In this state it is possible to switch the IOM interface to power down.
3. These transitions may be implemented for reasons of circuit simplification.

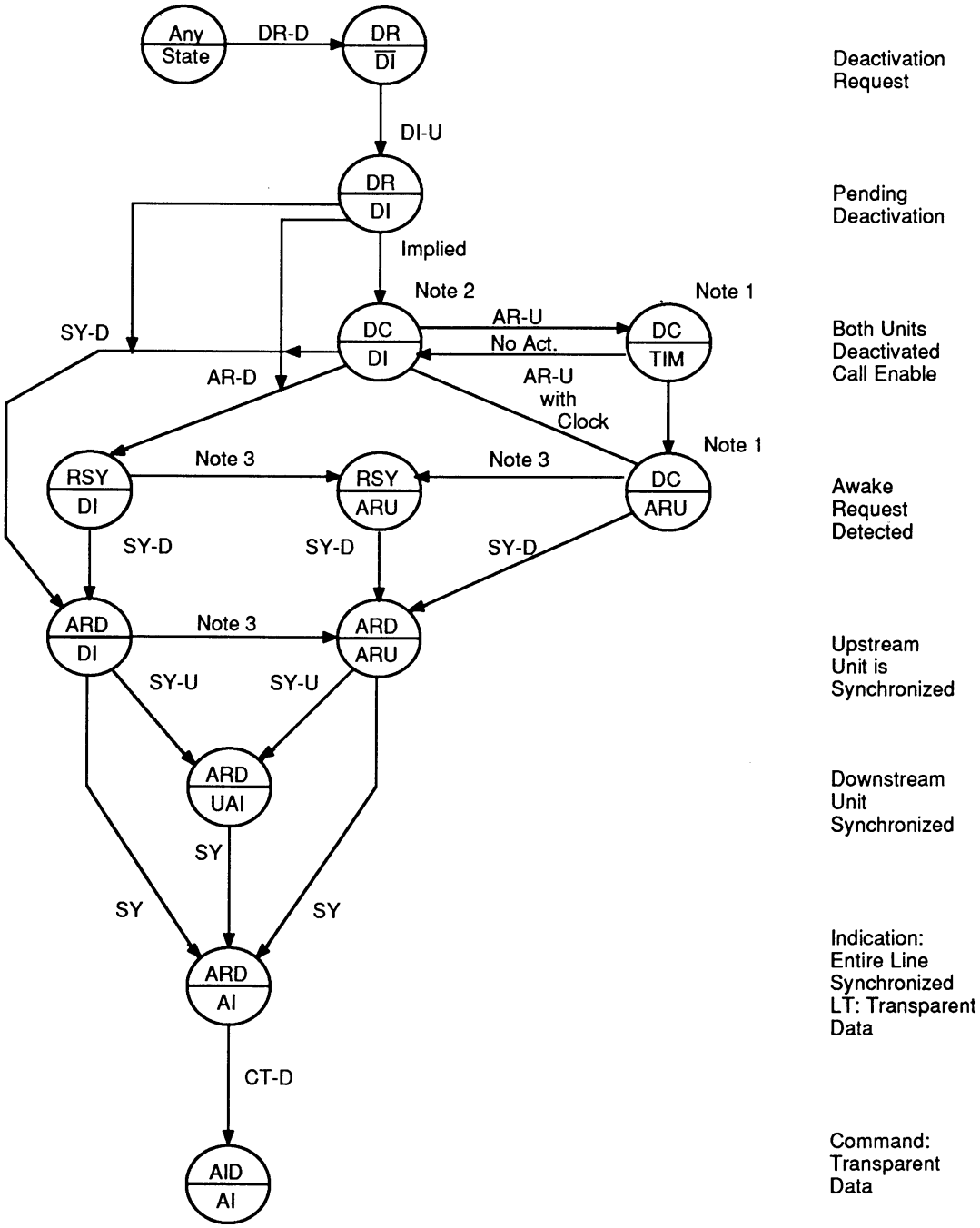
Figure 5-6 Activation/Deactivation Protocol for the IOM-2 Interface in the TE



* L2 = Layer 2

Notes: 1. PU is allowed instead of DC.
2. In this state it is possible to switch the IOM interface to power down.
3. These transitions may be implemented for reasons of circuit simplification.

Figure 5-7 **Activation/Deactivation Protocol for the IOM-2 Interface in the Line Repeater**



Notes: 1. PU is allowed instead of DC.
2. In this state it is possible to switch the IOM interface to power down.
3. These transitions may be implemented for reasons of circuit simplification.

CHAPTER 6

APPLICATIONS

In the following section, four application examples are presented that cover line cards, NT1 devices, and terminal equipment.

LINE CARD

Two ISDN line-card architectures are shown in Figures 6-1 and 6-2. The first example shows an 8-line card with the control functions local to the card. The second example is of a 32-line architecture where the control is centralized on one card, with the line transceivers located on separate cards (4 or 8 per card). The line-transceiver cards are non-intelligent, and connect to the controller via an IOM-2 bus.

8-LINE ISDN LINE CARD

It is often desirable to use a modular approach when designing a switch. This allows the capacity switch to be expanded in line-card-sized increments. Each line card contains the line transceivers, line-card controller, microprocessor, and usually the D-channel processors. The line transceivers and line-card controller are interconnected via the IOM-2 bus, operating in line-card mode.

Figure 6-1 Channel Line-Card Block Diagram

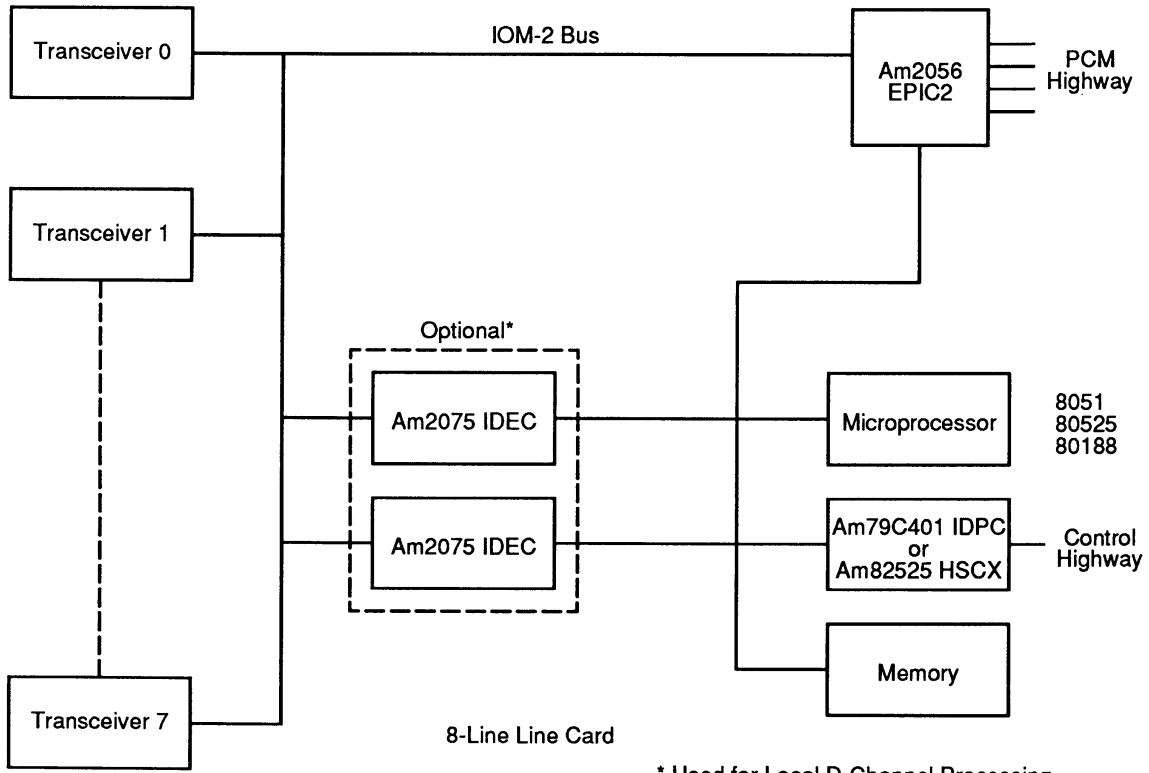


Figure 6-1 shows an example of this architecture. The line-card control function is performed by the Am2056 Extended PCM Interface Controller version 2 (EPIC), which is an 8-line version of the 32-line EPIC (Am2055) shown in the next example.

If the D channel is processed on the line card, two Am2075 ISDN Digital Exchange Controllers (IDEC™) are used. The IDEC is a quad-HDLC controller that can connect directly to the IOM-2 bus or the PCM Highway.

Connection to the switch's central controller is made via either the Am79C401 Integrated Data Protocol Controller (IDPC™), or the Am82525 High-Level Serial Communication Controller Extended (HSCX™). The IDPC is a single-channel device; the HSCX has two channels.

The type of microprocessor or microcontroller required depends on whether the D channel is processed on the line card or at a centralized location within the switch. If the D channel is processed locally, an 80188-class processor is required. If centralized D-channel processing is used, only an 8051-class microcontroller is required.

The architecture shown supports a range of line types, including the I.430 S interface and several U-interface protocols. One of the major benefits of this architecture is that a common software and hardware structure is used independent of the type of line transceiver. The key to this flexibility is that the line transceivers are not integrated with the D-channel processor. While it is practical to integrate the S transceiver with the D-channel processor, it is not practical to integrate a U transceiver with a D-channel processor. By integrating four D-channel processors in one integrated circuit, parts count and cost can be reduced while flexibility is retained.

32-LINE LINE CARD

In this example, the line transceivers are located on cards separate from the line-card control functions. This allows 32 lines of non-intelligent transceiver cards, partitioned by 1, 2, 4, or 8 transceivers per card, to share the overhead of the line-card controller, microprocessor, and intra-switch communication functions. Figure 6-2 is an example of a "by 8" organization.

The Am2055 EPIC provides four IOM-2 buses plus connection to up to four PCM Highways. The EPIC also allows B channels to be interconnected internally, thus providing the first layer of the switching hierarchy.

The D-channel processing function can be located on the controller board or at some central location within the switch.

As with the 8-line architecture, an Am79C401 IDPC or Am82525 HSCX provides the intra-switch communication link.

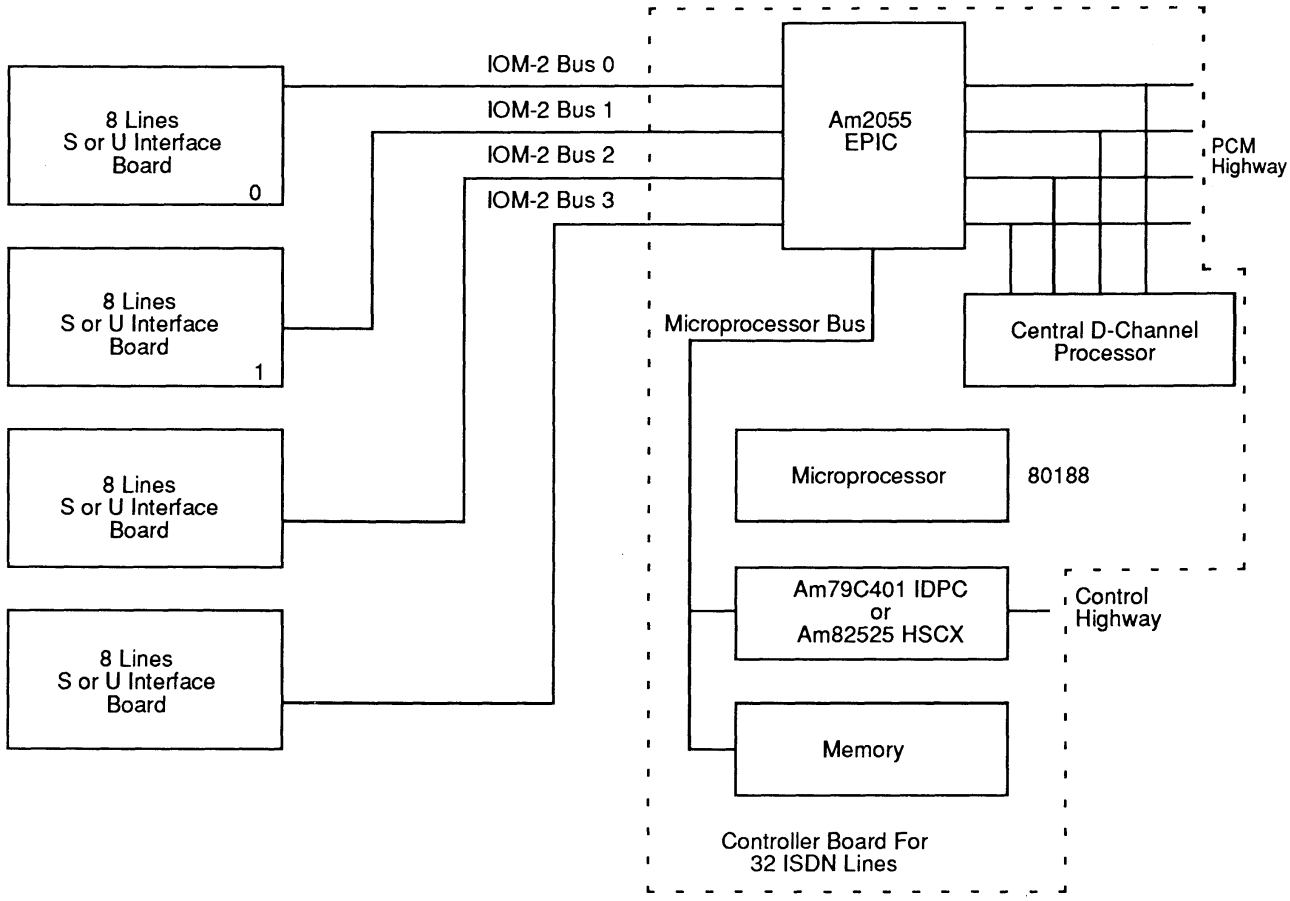
TERMINAL

The variety of types of ISDN terminal equipment is legion. One example is a terminal adapter that utilizes the V.110 rate adaptation protocol. Figure 6-3 shows a block diagram of such a terminal adapter using the Am79C30A Digital Subscriber Controller™ (DSC) and the Am2110 ISDN Terminal Adapter Circuit (ITAC™). The IDC and ITAC are connected via an IOM-2 bus operating in terminal mode. In this case, the IOM-2 bus is used to carry the B-channel data and network clock information (8-kHz frame rate carried via the SFC signal).

The Am79C30A DSC contains the S/T interface transceiver, codec, tone generator, analog interface, and D-channel protocol processor. The Am2110 ITAC provides the terminal interface (USART) and the V.110 protocol processor.

An 80C321 microcontroller provides the processing intelligence as well as an integrated watchdog timer.

Figure 6-2 32-Channel Line-Card Block Diagram



NT1

The Network Terminator type 1 (NT1) provides a U interface, two-wire, to T interface, four-wire, connection. In addition to terminating the interfaces and interconnecting the B and D channels, the NT1 performs network maintenance functions such as loop backs. As a result, the B, D, C/I, and monitor channels of the IOM-2 bus (terminal mode) are utilized.

An Am2081 S-Bus Circuit Extended (SBCX™) provides the T interface transceiver, and an Am2091 ISDN Echo Canceller (IEC™) provides the 2B1Q U interface transceiver. The two devices are connected via an IOM-2 terminal mode bus. The IEC is the upstream component, and the SBCX is the downstream component.

All inter-chip communication is handled over sub-frame 0 of the IOM-2 bus. The C/I channel (C/I0) is used to communicate line activation/deactivation requests and status information between the IEC and SBCX. The monitor channel (M0) is used to carry information from the network maintenance multiframe channels (S and Q bits of the T interface and the EOC bits of the 2B1Q U interface).

Figure 6-3 V.110 Terminal Adapter Block Diagram

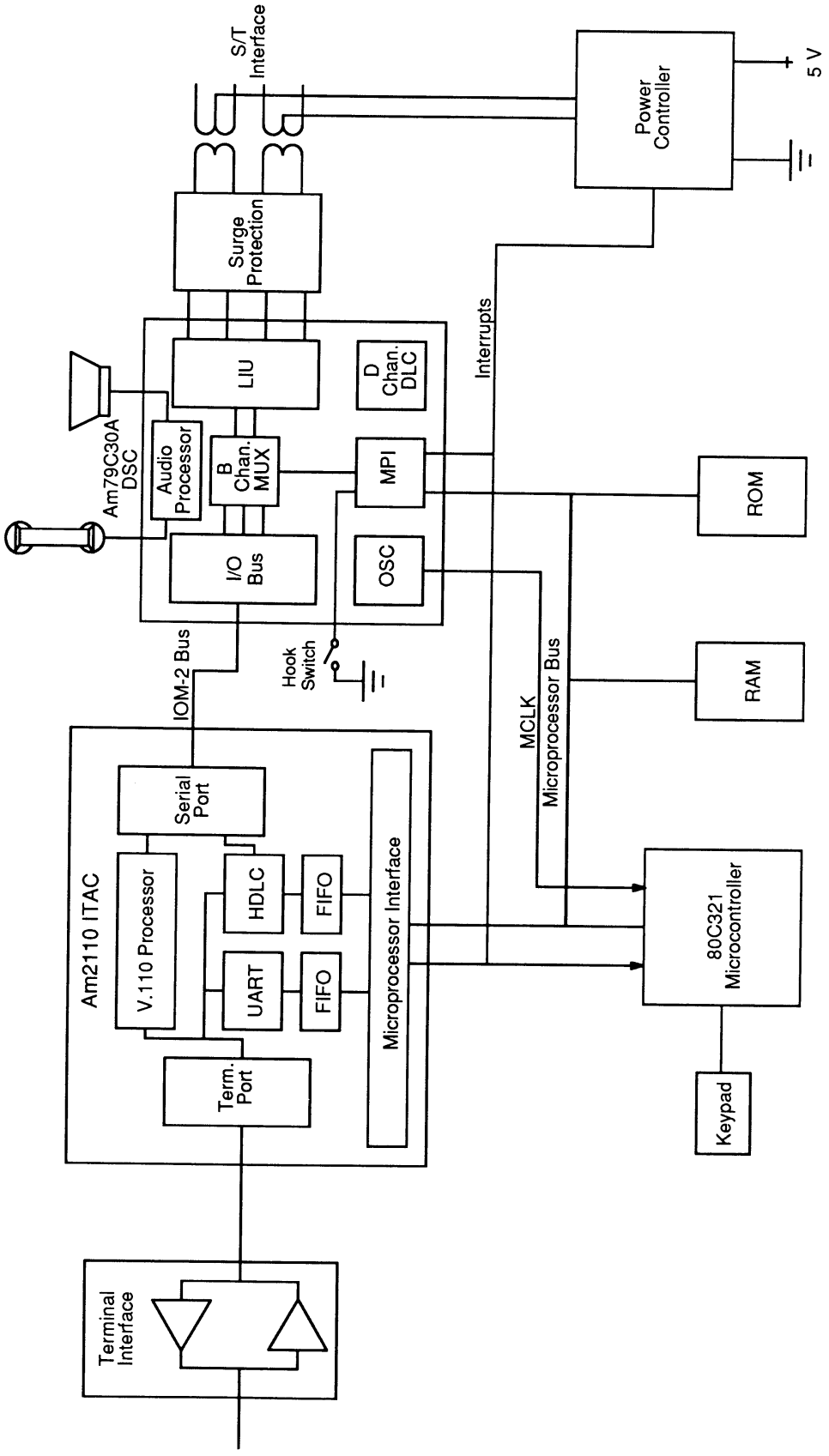
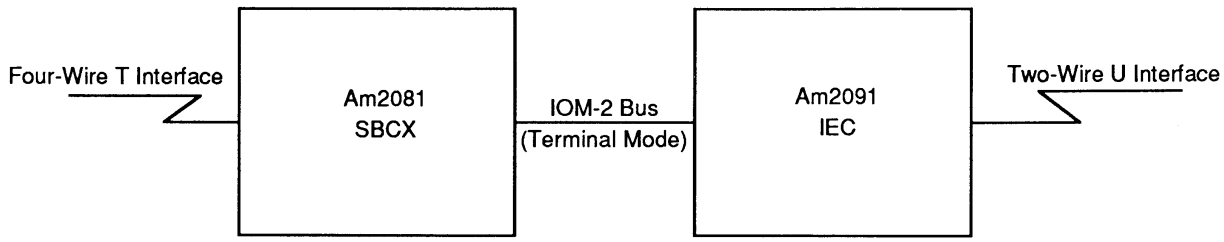


Figure 6-4 NT1 U Interface (2B1Q) to T Interface



CHAPTER 7

IOM-2 PIN DESCRIPTION

IOM-2 BUS PINS

The IOM-2 standard defines seven pins for data and clocks, three of which are only used in the terminal version. The pin names used in this document are generic; the actual pin names of specific devices may be different. Also, the data pins may be inputs, outputs, or bidirectional, depending on where the device is relative to the other devices on the IOM-2 bus. Refer to the "Pin Direction Reversal" section for more details.

DD, Data Downstream

Data from the network toward the subscriber. When the bus is deactivated, or when data is not being transmitted over a given channel, DD is held in a high state.

DU, Data Upstream

Data from subscriber toward the network. When the bus is deactivated, or when data is not being transmitted over a given channel, DU is held in a high state.

FSC, Frame Synchronization Clock

Eight-kHz clock indicating the start of a frame. FSC is always generated by the upstream device, which is the Layer 1 device in terminal applications, or the line-card controller in line-card applications.

DCL, Data Clock

DCL is used to clock data on to and off of the bus, and operates at twice the data rate. The clock rate is 16 kHz · N, where N is the number of sub-frames. There are three sub-frames (of four octets each) in the terminal mode, and from one to eight sub-frames in the line-card mode. DCL is always generated by the upstream component. When the bus is deactivated, DCL is held in a low state.

BCL, Bit-rate Clock (Terminal Mode Only)

BCL is a 1X clock running at 768 kHz. It is used as the data clock for non-IOM-2-compatible devices.

SDS1, SDS2, Serial Data Strobes 1 and 2 (Terminal Mode Only)

These active-high strobes are used by non-IOM-2 devices to specify or mark B (or IC) channels.

IOM-2 ADDRESS PINS

IOM-2-based ICs that do not have microprocessor interfaces require a means to designate bus addressing. For example, in an ISDN line-card application where eight line transceivers are connected to the line-card controller via the IOM-2 bus, each transceiver must know which sub-frame to use. This is normally handled with strapping pins on the transceiver or codec filter.

CHAPTER 8

ELECTRICAL AND SWITCHING CHARACTERISTICS

DC CHARACTERISTICS

Temperature Ambient = 0 to +70°C
Power Supply Range: V_{DD} = 5V ±0.25 V
GND = 0 V
External pull-up resistor required for each data line. D_{OUT} is an open drain output

Symbol	Parameter	Condition	Min.	Max.	Units
V_{IH}	High Level Input Voltage	Maximum Leakage Current = ±10 µA	2	V_{DD} +0.4	V
V_{IL}	Low Level Input Voltage	Maximum Leakage Current = ±10 µA	V_{SS} –0.4	0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = –0.4 mA	2.4		V
V_{OH}	High Level Output Voltage	I_{OH} = –0.2 mA	3.5		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA		0.45	V
V_{OL} D_{OUT}	Low Level Output Voltage D_{OUT}	I_{OL} = 7 mA		0.45	V
C	Input/Output Capacitance			10	pF
C_{OUT}	Load Capacitance			150	pF

AC TIMING

LINE-CARD TIMING

The IOM-2 line-card mode AC timing characteristics are given below.

TERMINAL TIMING

The IOM-terminal mode AC timing characteristics are given below.

Figure 8-1 Timing of the IOM-2 Interface

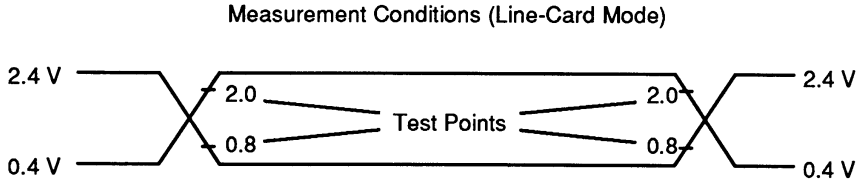
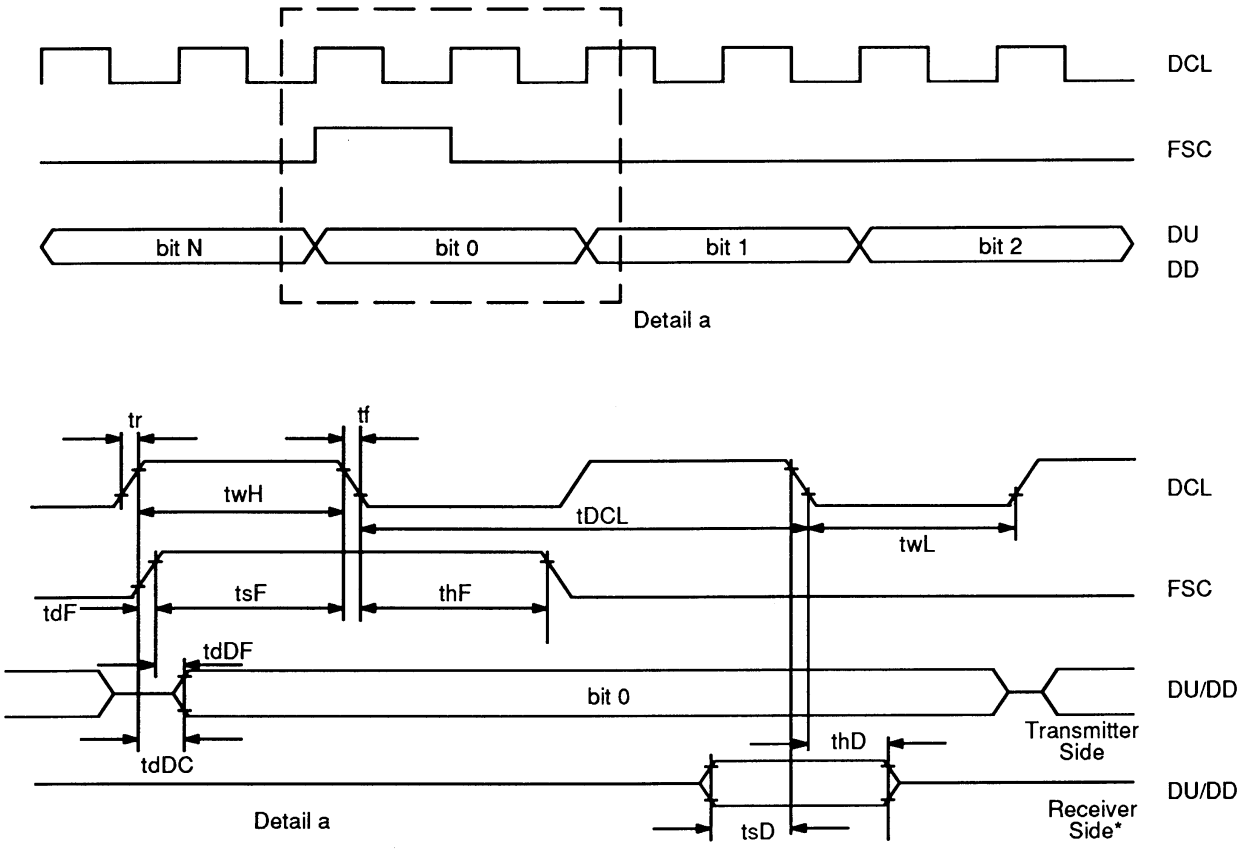


Figure 8-2 DCL, FSC, DU, and DD Characteristics



* Although the receiver side is not part of the interface specification, some typical values are given here.

Table 8-1 **Timing Characteristics of IOM-2 Interface**

Dynamic Characteristics: Slave*

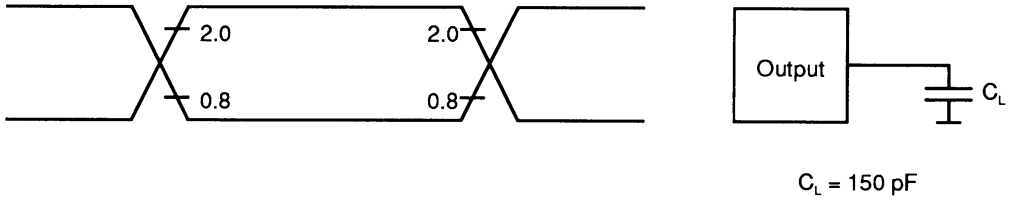
Parameter	Signal	Abbr.	Min.	Max.	Units
Data clock	DCL	tr, tf		60	ns
Clock period	DCL	TDCL	110		ns
Pulse width	DCL	twH, twL	53		ns
Frame sync	FSC			60	ns
Frame setup	FSC	tsF	70		ns
Frame hold	FSC	thF	40		ns
Data delay/clock	DOUT	tdDC		100[1]	ns
Data delay/frame	DOUT	tdDF		150[1]	ns
Data setup	DIN	tsD	twH + 20		ns
Data hold	DIN	thD	50		ns

Dynamic Characteristics: Master

Parameter	Signal	Abbr.	Test Conditions	Min.	Typ.	Max.	Units
Data clock	DCL	tr, tf	CL = 150 pF	50			ns
Clock period[2]	DCL	TDCL	OSC = $\pm 10^{-4}$	1800	1953	2100	ns
Pulse width[2]	DCL	twH, twL	OSC = $\pm 10^{-4}$	840			ns
Clock period[3]	DCL	TDCL	OSC = $\pm 10^{-4}$	239	244	249	ns
Pulse width[3]	DCL	twH, twL	OCL = $\pm 10^{-4}$	95	122		ns
Frame sync	FSC	tr, tf	CL = 150 pF			50	ns
Frame delay	FSC	tdF	CL = 150 pF	–twL		50	ns
Data delay/clock	DOUT	tdDC	CL = 150 pF			100	ns
Data setup	DIN	tsD		twH + 20			ns
Data hold	DIN	thD		50			ns

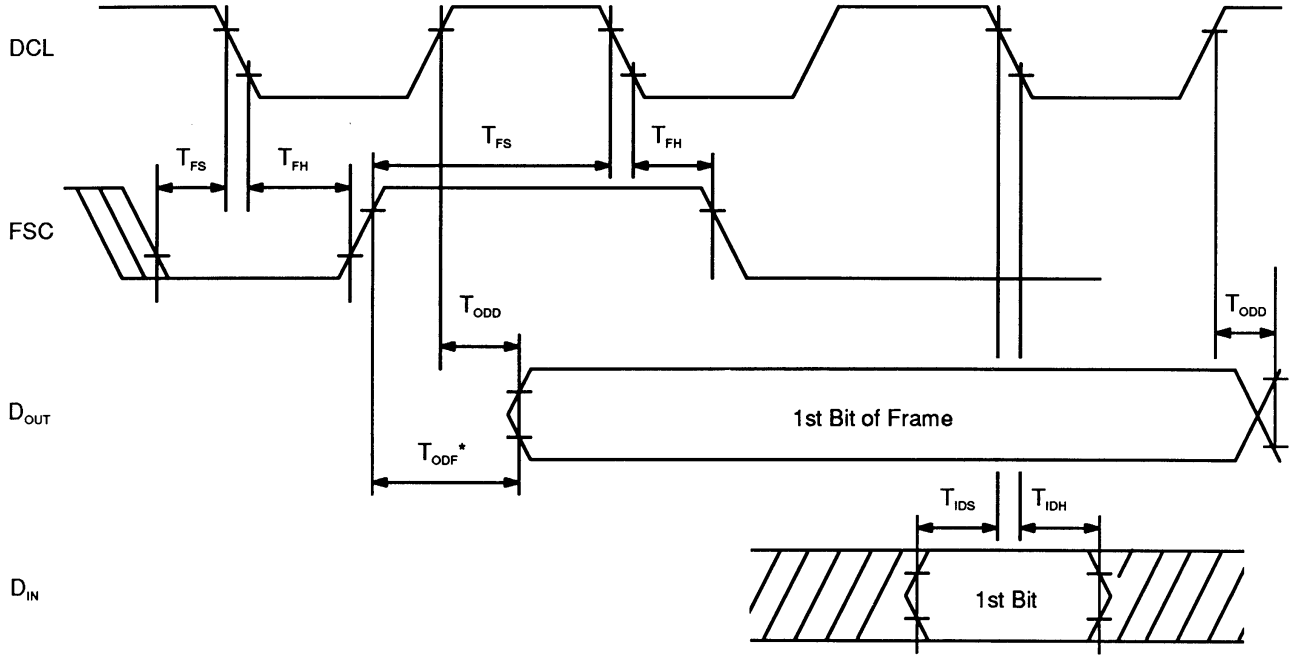
*Although the output timing is not part of the interface specification, some typical values are given here.
1. condition CL = 150 pf
2. 256 kb/s
3. 2.048 Mb/s

Figure 8-3 **Measurement Conditions (Terminal Mode)**



C_L = 150 pF

Figure 8-4 DCL, FSC Characteristics



* Each bit output on D_{OUT} shall be produced synchronously with respect to every other rising edge of DCL, except when a rising edge of FSC occurs later than T_{ODF}–T_{ODD} before the rising edge of DCL. In this case, the first bit of the frame can be output at T_{ODF} after the rising edge of FSC, if FSC causes a change in the internal frame bit counter of the slave device.

Table 8-2 DCL, FSC Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
T_{FS}	Frame sync setup		70		ns
T_{FH}	Frame sync hold		40		ns
T_{IDS}	Input data setup		TWH + 50		ns
T_{IDH}	Input data hold (High impedance to active or active to high impedance)		50		ns
T_{ODD}	Output data delay	CL = 150 pF		150*	ns
T_{ODF}	First bit of frame from frame sync	CL = 150 pF		150*	ns

*See Figure 8-6—DCL, BCL Characteristics.
**These times are not the object of this specification and are only typical values.

Figure 8-5 **BCL, SDS Characteristics**

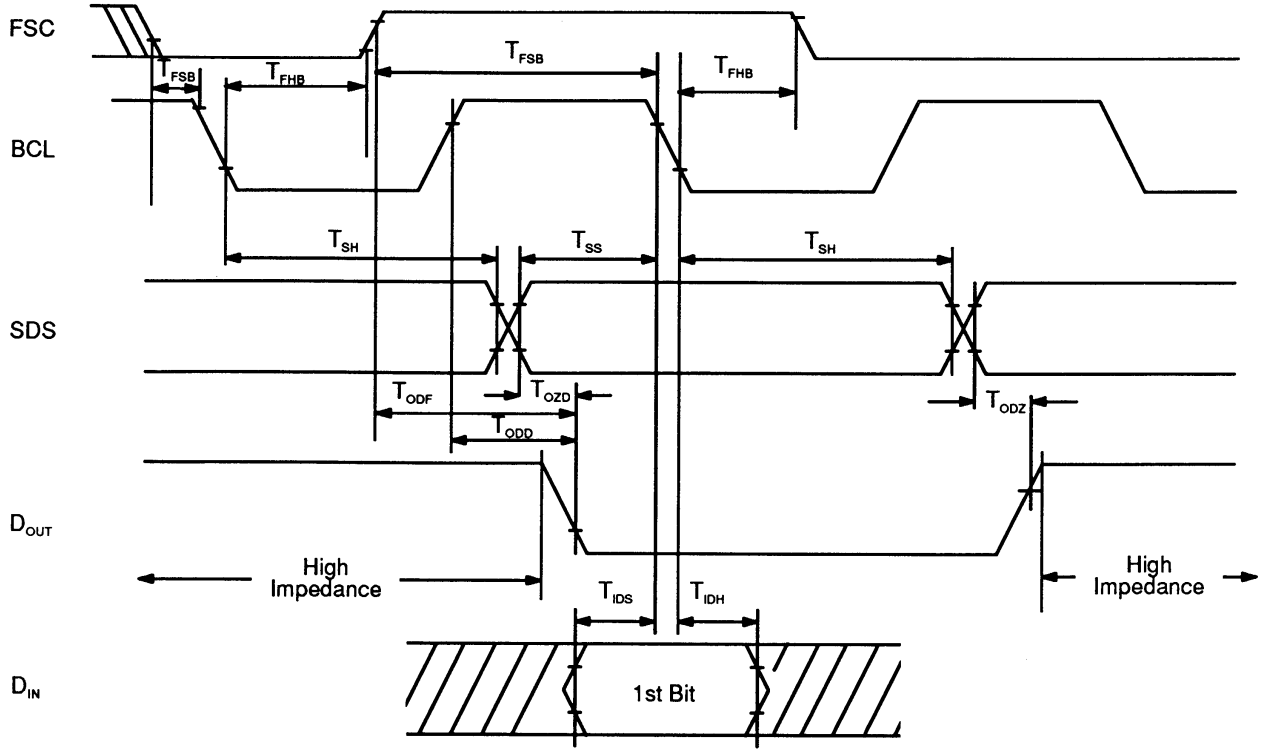


Table 8-3 **BCL, SDS Dynamic Characteristics**

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
T_{FSB}	Frame sync set-up to BCL		70		ns
T_{FHB}	Frame sync hold from BCL		40		ns
T_{SH}	Strobe signal hold		40		ns
T_{SS}	Strobe signal setup		100		ns
T_{IDS}	Input data setup		50		ns
T_{IDH}	Input data hold		50		ns
T_{OZD}	Output data high impedance-to-active from strobe	CL = 150 pF		150*	ns
T_{ODZ}	Output data active-to-high impedance from strobe	CL = 150 pF		150*	ns
T_{ODD}	Output data delay	CL = 150 pF		100*	ns
T_{ODF}	First bit from frame sync			150*	ns

*These times are not the object of this specification, and are only typical values.

DCL, BCL Characteristics

The DCL and BCL clocks may have a jitter such that a period may be either reduced or extended at most once every 12.5 µs. This reduction (or extension) may be done by reducing (or extending) either the high or the low phase. The sum of the absolute values of phase jumps during any 250-µs time interval shall not exceed 163 ns.

Figure 8-6 **DCL, BCL Characteristics**

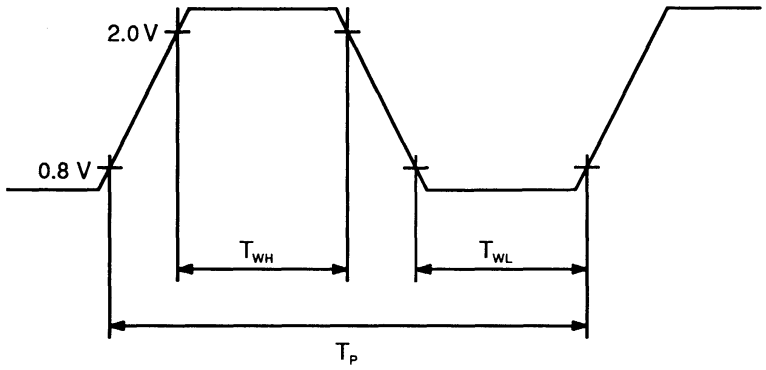


Table 8-4 **DCL, BCL Characteristics for DCL = 1536 kHz**

Symbol	Signal	Parameter	Min.	Typ.	Max.	Units
T_p	DCL	Clock period	487	651	815	ns
T_{WH}	DCL	Clock width high	120		532	ns
T_{WL}	DCL	Clock width low	120		532	ns
T_p	DCL	Clock period	1138	1302	1466	ns
T_{WH}	BCL	Clock width high	445		857	ns
T_{WL}	BCL	Clock width low	445		857	ns

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